IMPLEMENTING SHA-224/256 ALGORITHM FOR SECURE COMMITMENT SCHEME APPLICATIONS USING FPGA

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I. INTRODUCTION

SHS (Secure Hash Standard) is a hash algorithm (FIPS PUB 180-1), released by United States National Institute of Standards and Technology (NIST) in 1995. Because the algorithm is collision-resistant and non-reversible, it is widely used in the information security field at present, which are more well-known SSL, IPSec and PKCS. But as people study the algorithm in-depth, its security has also been questioned and threatened[1][2]. This has prompted NIST release the latest SHS specifications (FIPS PUB 180-3) in October 2008. With the previous version (FIPS PUB 180-2 CHANGE NOTICE, August 2002), the biggest difference is that SHA-224 algorithm has been formally included in the SHS standard. Because SHA algorithm itself is a very complex algorithm, its calculation is to a larger quantity, and each iteration needs to rely on the previous calculation, it is often used hardware implementation to increase the processing speed[3]. This paper uses the similarity between SHA-224 and SHA-256 algorithm and hardware description language to design and implement the time division multiplexing SHA-224/256 IP core. The IP core will not only be able to generate digital signature to protect the information integrity and security, but also generate the double-key of 3DES algorithm to provide a more reliable, safe, and convenient keys. So it has a broad application prospects. A typical application of SHA in the digital signature algorithm is shown in Fig.1.

II. COMPUTER BUS MEMORY SYSTEM DESIGN

SHA-224 and SHA-256 are the two kinds of algorithms in the SHS standard (FIPS PUB 180-3). They can handle input messages whose length is less than $2^{64}$ bits, but the outputs are separately compressed into 224 bits and 256 bits. SHA-224 algorithm and SHA-256 algorithm have only two differences: first, the initialized hash values are different; second, the results of SHA-224 are needed to be truncated.

SHA-256 algorithm has two steps to complete the calculation. The first step is to preprocess the input message to be filled and divided, generating 512 bits blocks. The second step is to calculate the hash value, that is to say, every block operates to produce the final results. After dividing blocks, every block messages can be processed by the following methods. And the details are described in reference [4].

1) Giving $K_0$, $K_1$, ..., $K_63$ sixty-four 32-bits K the initial value.

2) Giving $H_0$, $H_1$, $H_2$, $H_3$, $H_4$, $H_5$, $H_6$, $H_7$ eight 32-bits variables the specified initial hash values. Every block messages is to do the from step (3) to(7).

3) Divide the 512bits block into sixteen 32-bits words $W_0$, $W_1$, ..., $W_{15}$.

4) For $i = 16$ to 63
after receiving the value, key value, and the values of the input and parallel computing architecture will be used to achieve the time division multiplexing of the parallel architecture. The multiplexing of IP core, a group of registers is used to achieve the time-division multiplexing of SHA-224 and SHA-256 algorithms.

As can be seen from the description of the algorithm, the core of the whole algorithm is the second step calculating the hash values. The first step can be achieved by the upper software. Therefore, several issues need to be solved for the calculation of hash values.

△ Determine the data bus width. Because the message length handled by the algorithm is variable, the external data bus width and the corresponding control core. From the third step and sixth step of the algorithm, the relationship between production and consumption among them entirely can be handled by the parallel architecture.

△ The multiplexing of IP core, a group of registers is used to achieve the time-division multiplexing of SHA-224 and SHA-256 algorithms.

△ Performance and area optimization, pipelining and parallel computing architecture will be used to design simple structure and fast IP core.

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Every sub-module of the entire IP core is designed according to the data flow of the SHA-256 algorithm.

First, determine the interfaces of the IP core. Considering the portability of the IP core, 32-bits data bus and 11-bits control bus. Control bus includes clock signal, reset signal, control enable signal, function selection signal, control signal and state signal. Next, According the relationship between production and consumption of data flow, the IP core can be divided into the Data pool, ALU(Arithmetic Logic Unit), Register files and Counter four parts(shown in Fig.2). Data pool is used to save the constant and Wi in the algorithm, including the initial hash value, key value, and the values of the input words and the expansion words. ALU is used to complete the arithmetic and logic operations. Register files are used as the dedicated registers to save the values of a, b, c, d, e, f, g, h. Counter is added 1 in every clock rising edge arrives to meet the iterative control.

When input the corresponding data and control signal to the IP core, the IP core does iterative processing in a block (512 bits).

The counter is cleared after every 64 clocks to maintain synchronization between itself and the word. Its data flow is the following: Data pool gives Wt and Kt under the control of the Counter and sends them to ALU. ALU does the corresponding arithmetic and logic operations after receiving the data, and save the results to register files until the end of this iteration. At the beginning, the blocks, the words and the end, the Register files you need to provide the corresponding results for ALU or the output bus under the control of external control signals and the Counter.

A. Data pool

The Data pool consists of look-up table unit and shift register unit. Look-up table unit is responsible for...
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TABLE I. SYNTHESIS RESULTS

<table>
<thead>
<tr>
<th>Project name</th>
<th>Total logic elements</th>
<th>Total flip-flops</th>
<th>Total memory bits</th>
<th>Total logic elements</th>
<th>Total flip-flops</th>
<th>Total memory bits</th>
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</thead>
<tbody>
<tr>
<td></td>
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<td>1,124</td>
<td>4,073</td>
<td>2,646</td>
<td>1,154</td>
<td>4,073</td>
</tr>
</tbody>
</table>

IV. SYNTHESIS AND SIMULATION

In this design, this IP core is described by Verilog HDL language and has been implemented to FPGA Altera Cyclone EP2C35F672C6. Then it is synthesized and routed on the QuartusII 8.0. Finally it is simulated by ModelSim[7] to test if the IP core is correct.

A. Synthesis results

Table 1 shows the comparison data whether or not using the CSA adder (Default comprehensive option), in which the performance is increased by 26% and the resource consumption is also increased by 26% after using the CSA adder. Taking into account the internal structure of FPGA, using the HardCopy technology [8] turns the IP core to ASIC achieving that the power consumption will be further reduced and the performance and speed will be increased by almost 50% [9].

B. Timing simulation

Under that the simulation clock is 100MHz, its simulation waveforms are shown in Fig.3 (SHA-224) and Fig.4 (SHA-256), in which the input test string is 12345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123456789012345678901234567890123
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V. CONCLUSION

This paper uses the similarity between SHA-224 and SHA-256 algorithms to design a time division multiplexing IP core. 32-bits data bus makes this design has a friendly data interface, and the whole design has a simple hardware structure and fast running speed and can be widely used in digital signatures and 3DES key generation systems.

REFERENCES


[7] Jiang Hao, Li Zheying. FPGA design flow based on a variety