Fall 10-7-2012

Proceeding of International Conference On Eletrical,Electronics,Computational Vision and Robotics ICEECVR-2012

Prof. (Dr.) Srikanta Patnaik

Editorial

Inventions and discoveries have emanated from creative minds that have been constantly working and imaging the outcome in the mind. With imaging and constant effort, all the forces of the Universe work for that inspired mind, thereby leading to inventions or discoveries. Higher the number of creative minds in an organization, the best results of invention and discoveries will emerge. Unique academic environment results into great thinking that leads to creativity.

Mobile Operators around the world are enjoying the fruits of the rapid growth in mobile broadband, which was a challenge before the Engineers. Before talking about challenges, one should first recognize that the data boom is a huge opportunity for the entire mobile industry. Customers are still willing to pay a reasonable amount for access to the services, products and content carried by mobile networks. However, it is true that the growth has been so fast and so big that it has created tension on infrastructure. The new devices and applications behave in a way that is often not optimized for mobile networks. Many applications on smartphones for instance are almost always alive and exchanging information with the network even when the customer is not actively using them. They create an ever present noise in the form of signaling that can stress the network. The researchers have to cope with this by Hybridizing several technologies, including HSPA, LTE and WLAN, to create the access capacity necessary to provide the best broadband coverage everywhere. HSPA should be pushed to ever higher bandwidths and introduce LTE to WLAN proposition to build coverage. It also needs to develop all the engineering behind that backhaul. Technicians has to work with vendors to collectively, invest in new and resilient architectures for developing the networks. It can be new systems and network architectures that will allow for separate dimensioning of traffic and signaling. But that's not the whole story. There is a need to work with the developer community to help them design their applications to work more intelligently with the networks. It is in their interest that their applications are more efficient and can deliver a better experience on smartphones and tablets for the customer's benefit.

Smart grids electricity transmission and distribution that uses two-way communications to optimize supply and demand which are vital in managing energy consumption, integrating renewable and micro power generation, and supporting the greater use of electric vehicles. The benefits of smart grids could be substantial. In the United States alone, successful deployment of smart grid technologies could yield savings to society of USD 130 billion annually,that claims a recent McKinsey magazine. The deployment of smart metering is already well advanced in Finland, Italy, Sweden and California. Smart meters provide information for utilities to measure energy consumption in real time and for customers to follow the amount and cost of their consumption. Trials have shown

that peak loads can be reduced by 20% simply by making consumption data available to consumers. Therefore it is rightly said:-

"**Discovery consists of seeing what everybody has seen and thinking what nobody has thought."**
Albert Von Szent-Gyorgy

So this conference has been designed to stimulate the young minds including Research Scholars, Academicians, and Practitioners to contribute their ideas, thoughts and nobility in these disciplines of engineering. It is a pleasure to welcome all the participants, delegates and organizer to this International Conference on behalf of IOAJ family members. This conference has received a great response from all parts of the country and abroad for the presentation and publication in the proceedings.

I sincerely thank all the authors for their valuable contribution to this conference. I am indebted towards the reviewers and Board of Editors for their generous gifts of time, energy and effort.

Editor-in-Chief

Prof. (Dr.) Srikanta Patnaik
Chairman, I.I.M.T., Bhubaneswar
Intersceince Campus,
At/Po.: Kantabada, Via-Janla, Dist-Khurda
Bhubaneswar, Pin:752054. Orissa, INDIA.

ADVANCED DIRECT POWER CONTROL OF MATRIX CONVERTER BASED UNIFIED POWER-FLOW CONTROLLER

K.MEENENDRANATH REDDY , O.HEMAKESAVULU & M. PADMA LALITHA

Department of Electrical Engg, P.G Student, AITS College, Rajampeta,

Abstract— An electrical power system is a large interconnected network that requires a careful design to maintain the system with continuous power flow operation without any limitations. Flexible Alternating Current Transmission System (FACTS) is an application of a power electronics device to control the power flow and to improve the system stability of a power system. This paper presents a direct power control (DPC) for three-phase matrix converters operating as unified power flow controllers (UPFCs). Matrix converters (MCs) allow the direct ac/ac power conversion without dc energy storage links; therefore, the MC-based UPFC (MC-UPFC) has reduced volume and cost, reduced capacitor power losses, together with higher reliability. Theoretical principles of direct power control (DPC) based on sliding mode control techniques are established for an MC-UPFC dynamic model including the input filter. As a result, line active and reactive power, together with ac supply reactive power, can be directly controlled by selecting an appropriate matrix converter switching state guaranteeing good steady-state and dynamic responses. Experimental results of DPC controllers for MC-UPFC show decoupled active and reactive power control, zero steady-state tracking error, and fast response times. Compared to an MC-UPFC using active and reactive power linear controllers based on a modified Venturini high-frequency PWM modulator, the experimental results of the advanced DPC-MC guarantee faster responses without overshoot and no steady-state error, presenting no cross-coupling in dynamic and steady-state responses.

Index Terms— *Direct power control (DPC), matrix converter (MC), unified power-flow controller (UPFC).*

I. INTRODUCTION

The technology of power system utilities around the world has rapidly evolved with considerable changes in the technology along with improvements in power system structures and operation. The ongoing expansions and growth in the technology, demand a more optimal and profitable operation of a power system with respect to generation, transmission and distribution systems. In the present scenario, most of the power systems in the developing countries with large interconnected networks share the generation reserves to increase the reliability of the power system. However, the increasing complexities of large interconnected networks had fluctuations in reliability of power supply, which resulted in system instability, difficult to control the power flow and security problems that resulted large number blackouts in different parts of the world. The reasons behind the above fault sequences may be due to the systematical errors in planning and operation, weak interconnection of the power system, lack of maintenance or due to overload of the network.

In order to overcome these consequences and to provide the desired power flow along with system stability and reliability, installations of new transmission lines are required. However, installation of new transmission lines with the large interconnected power system are limited to some of the factors like economic cost, environment related issues. These complexities in installing new transmission lines in a power system challenges the power engineers to research on the ways to increase the power flow with the existing transmission line without reduction in system stability and security. In this research process, in the late 1980's the Electric Power Research Institute (EPRI) introduced a concept of technology to improve the power flow, improve the system stability and reliability with the existing power systems. This technology of power electronic devices is termed as Flexible Alternating Current Transmission Systems (FACTS) technology. It provides the ability to increase the controllability and to improve the transmission system operation in terms of power flow, stability limits with advanced control technologies in the existing power systems.

In the last few decades, an increasing interest in new converter types, capable of performing the same functions but with reduced storage needs, has arisen. These converters are capable of performing the same ac/ac conversion, allowing bidirectional power flow, guaranteeing near sinusoidal input and output currents, voltages with variable amplitude, and adjustable power factor. These minimum energy storage ac/ac converters have the capability to allow independent reactive control on the UPFC shunt and series converter sides, while guaranteeing that the active power exchanged on the UPFC series connection is always supplied/absorbed by the shunt connection. Conventional UPFC controllers do not guarantee robustness.

In the dependence of the matrix converter output voltage on the modulation coefficient was investigated, concluding that MC-UPFC is able to control the full range of power flow. Recent nonlinear approaches enabled better tuning of PI controller parameters.

Still, there is room to further improve the dynamic response of UPFCs, using nonlinear robust controllers. In the last few years, direct power control techniques have been used in many power applications, due to their simplicity and good performance

In this paper, a matrix converter- based UPFC is proposed, using a direct power control approach (DPC-MC) based on an MC-UPFC dynamic model. In order to design UPFCs, presenting robust behavior to parameter variations and to disturbances, the proposed DPC-MC control method is based on sliding mode-control techniques, allowing the real-time selection of adequate matrix vectors to control input and output electrical power. Sliding mode-based DPC-MC controllers can guarantee zero steady-state errors and no overshoots, good tracking performance, and fast dynamic responses, while being simpler to implement and requiring less processing power, when compared to proportional-integral (PI) linear controllers obtained from linear active and reactive power models of UPFC using a modified Venturini high-frequency PWM modulator.

The dynamic and steady-state behavior of the proposed DPC-MC P, Q control method is evaluated and discussed using detailed simulations and experimental implementation. Simulation and experimental results obtained with the nonlinear DPC for matrix converter-based UPFC technology show decoupled series active and shunt/series reactive power control, zero steady-state error tracking, and fast response times, presenting faultless dynamic and steady-state responses.

II. MODELING OF THE MATRIX CONVERTER UPFC POWER SYSTEM

A. General Architecture

A simplified power transmission network using the proposed matrix converter UPFC is presented in Fig. 1, where V_S and V_R are, respectively, the sending-end and receiving-end sinusoidal voltages of the G_S and G_R generators feeding load Z_L . The matrix converter is connected to transmission line 4, represented as a series inductance with series resistance (L_2 and R_2), through coupling transformers and T_1 and T_2 . Fig. 2 shows the simplified three-phase equivalent circuit of the matrix UPFC transmission system model. For system modeling, the power sources and the coupling transformers are all considered ideal.

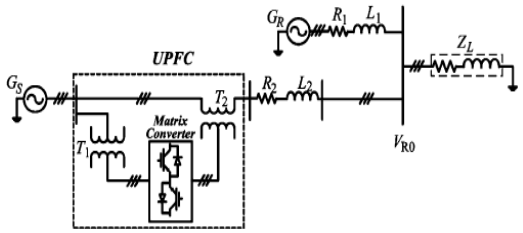


Fig. 1. Transmission network with matrix converter UPFC.

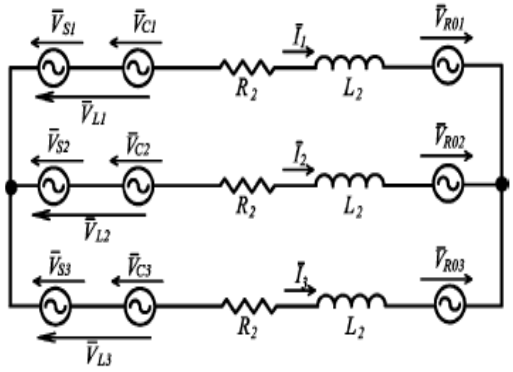


Fig. 2. Three-phase equivalent circuit of the matrix UPFC and transmission line.

A matrix converter is a direct frequency changer. This converter consists of an array of n×m bidirectional switches arranged so that any of the output lines of the converter can be connected to any of the input lines. The bidirectional switch is realized by using some semiconductor devices. They can be either discrete or integrated to the module. The bidirectional switch can be implemented in various ways. For the matrix converter, we chose modules which include 3 bidirectional switches in common emitter a configuration. The modulator is thus realized for these switchers.

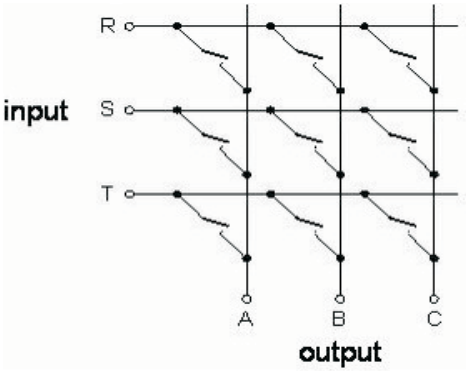


Fig. 3: Matrix converter 3×3

The Matrix Converter is a single stage converter which has an array of m× n bidirectional power switches to connect, directly, an m-phase voltage source to an n-phase load. The Matrix Converter of 3× 3 switches, shown in Figure5, has the highest practical interest because it connects a three-phase voltage source with a three-phase load, typically a

motor. Normally, the matrix converter is fed by a voltage source and for this reason, and the input terminals should not be short-circuited.

On the other hand, the load has typically an inductive nature and for this reason an output phase must never be opened. Defining the switching function of a single switch as

$$Skj = \begin{cases} 1, \text{Switch Skj closed} \\ 0, \text{Switch Skj open} \end{cases}$$

$$k = \{A\ B\ C\} \qquad j = \{a\ b\ c\}$$

The constraints discussed above can be expressed by

$$SAj + SBj + SCj = 1, \qquad j = \{a\ b\ c\}$$

With these restrictions, the 3× 3 Matrix Converter has 27 possible switching states.

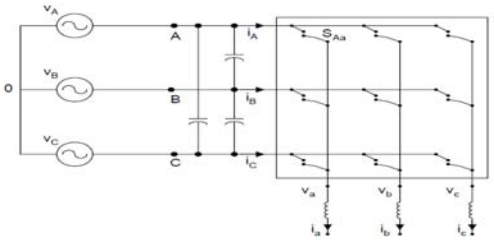


FIGURE 4: Simplified circuit of a 3× 3 Matrix Converter.

The load and source voltages are referenced to the supply neutral, '0' in the Figure 4, and can be expressed as vectors defined by:

$$V_o = \begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix}, \quad V_i = \begin{bmatrix} v_A(t) \\ v_B(t) \\ v_C(t) \end{bmatrix}$$

The relationship between load and input voltages can be expressed as:

$$\begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ba} & S_{Ca} \\ S_{Ab} & S_{Bb} & S_{Cb} \\ S_{Ac} & S_{Bc} & S_{Cc} \end{bmatrix} \begin{bmatrix} v_A(t) \\ v_B(t) \\ v_C(t) \end{bmatrix}$$

$$Vo = T \times Vi$$

Where *T* is the instantaneous transfer matrix.
In the same form, the following relationships are valid for the input and output currents:

$$i_i = \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} \qquad i_o = \begin{bmatrix} i_A(t) \\ i_B(t) \\ i_C(t) \end{bmatrix}$$

$$i_i = T^T \cdot io$$

Where T_T is the transpose matrix of T.

The above gives the instantaneous relationships between input and output quantities. To derive modulation rules, it is also necessary to consider the switching pattern that is employed. This typically follows a form similar to that shown in the Figure 5.

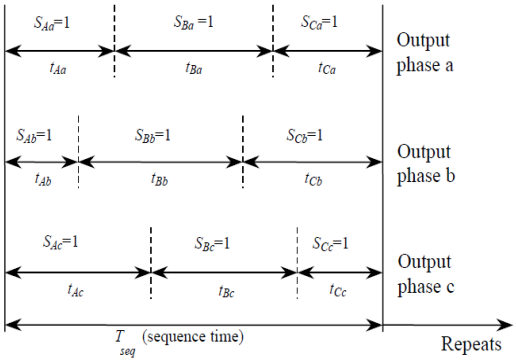


FIGURE 5: General form of switching pattern.

By considering that the bidirectional power switches work with high switching frequency, a low frequency output voltage of variable amplitude and frequency can be generated by modulating the duty cycle of the switches using their respective switching functions. Let $M_{kj}(t)$ be the duty cycle of switch $S_{kj}(t)$, defined as $M_{kj}(t) = t_{kj}/T_{seq}$, which can have the following values:

$$0 < Mkj(t) < 1, \qquad k = \{A\ B\ C\}, \quad j = \{a\ b\ c\}$$

The low-frequency transfer matrix is defined by

$$M(t) = \begin{bmatrix} M_{Aa} & M_{Ba} & M_{Ca} \\ M_{Ab} & M_{Bb} & M_{Cb} \\ M_{Ac} & M_{Bc} & M_{Cc} \end{bmatrix}$$

The low-frequency component of the output phase voltage is given by

$$Vo(t) = M(t)\ .\ Vi(t)$$

The low-frequency component of the input current is

$$i_i(t) = M(t)^T \cdot io(t)$$

The Matrix Converter is a forced commutated converter which uses an array of controlled bidirectional switches as the main power elements to create a variable output voltage system with unrestricted frequency. It does not have any dc-link circuit and does not need any large energy storage elements. The matrix converter is an array of bidirectional switches as the main power elements, which interconnects directly the power supply to the load, without using any dc-link or large energy storage elements.

The most important characteristics of matrix converters are; 1) Simple and compact power circuit, 2) Generation of load voltage with

arbitrary amplitude and frequency, 3) Sinusoidal input and output currents, 4) Operation with unity power factor, 5) Regeneration capability.

These highly attractive characteristics are the reason for the tremendous interest in this topology. The key element in a matrix converter is the fully controlled four quadrant bidirectional switch, which allows high frequency operation. The early work dedicated to unrestricted frequency changers used thyristors with external forced commutation circuits to implement the bi-directional controlled switch. With this solution the power circuit was bulky and the performance was poor. The introduction of power transistors for implementing the bidirectional switches made the matrix converter topology more attractive. However, the real development of matrix converters starts with the work of Venturini and Alesina published in 1980. They presented the power circuit of the converter as a matrix of bi-directional power switches and they introduced the name "Matrix Converter." One of their main contributions is the development of a rigorous mathematical analysis to describe the low-frequency behavior of the converter, introducing the "low frequency modulation matrix" concept. In their modulation method, also known as the direct transfer function approach, the output voltages are obtained by the multiplication of the modulation (also called transfer) matrix with the input voltages.

B. DIRECT POWER CONTROL OF MC-UPFC

I. Line Active and Reactive Power Sliding Surfaces

The DPC controllers for line power flow are here derived based on the sliding mode control theory. In steady state, V_d is imposed by source Vs. The transmission-line currents can be considered as state variables with first-order dynamics dependent on the sources and time constant of impedance L_2/R_2. Therefore, transmission-line active and reactive powers present first-order dynamics and have a strong relative degree of one, since from the control viewpoint, its first time derivative already contains the control variable (the strong relative degree generally represents the number of times the control output variable must be differentiated until a control input appears explicitly in the dynamics). From the sliding mode control theory, robust sliding surfaces to control the P and Q variables with a relatively strong degree of one can be obtained considering proportionality to a linear combination of the errors of the state variables. Therefore, define the active power error e_p and the reactive power error e_q as the difference between the power references P_{ref}, Q_{ref} and the actual transmitted powers P, Q, respectively.

$$e_P = P_{\text{ref}} - P$$
$$e_Q = Q_{\text{ref}} - Q.$$

Then, the robust sliding surfaces $S_p(e_p, t)$ and $S_Q(e_q,t)$ must be proportional to these errors, being zero after reaching sliding mode.

$$S_P(e_P,t) = k_P(P_{\text{ref}} - P) = 0$$
$$S_Q(e_Q,t) = k_Q(Q_{\text{ref}} - Q) = 0.$$

The proportional gains K_p and K_q are chosen to impose appropriate switching frequencies.

II. Line Active and Reactive Power Direct Switching Laws:-

The DPC uses a nonlinear law, based on the errors e_p and e_q to select in real time the matrix converter switching states (vectors). Since there are no modulators and/or pole zero-based approaches, high control speed is possible. To guarantee stability for active power and reactive power controllers, the sliding-mode stability conditions must be verified

$$S_P(e_P,t)\dot{S}_P(e_P,t) < 0$$
$$S_Q(e_Q,t)\dot{S}_Q(e_Q,t) < 0.$$

To design the DPC control system, the six vectors will not be used, since they require extra algorithms to calculate their time-varying phase. The variable amplitude vectors, only the 12 highest amplitude voltage vectors are certain to be able to guarantee the previously discussed required levels of V_{Ld} and V_{Lq} needed to fulfill the reaching conditions. The lowest amplitude voltages vectors, or the three null vectors could be used for near zero errors. If the control errors e_p and e_Q are quantized using two hysteresis comparators, each with three levels (-1, 0 and+1), nine output voltage error combinations are obtained. If a two-level comparator is used to control the shunt reactive power, as discussed in next subsection, 18 error combinations (9x2=18) will be defined, enabling the selection of 18 vectors. Since the three zero vectors have a minor influence on the shunt reactive power control, selecting one out 18 vectors is adequate. Using the same reasoning for the remaining eight active and reactive power error combinations and generalizing it for all other input voltage sectors, Table II is obtained. These P, Q controllers were designed based on control laws not dependent on system parameters, but only on the errors of the controlled output to ensure robustness to parameter variations or operating conditions and allow system order reduction, minimizing response times.

III. DIRECT CONTROL OF MATRIX CONVERTERS INPUT REACTIVE POWER:-

In addition, the matrix converter UPFC can be controlled to ensure a minimum or a certain desired reactive power at the matrix converter input. Similar to the previous considerations, since the voltage source input filter dynamics has a strong relative degree of two, then a suitable sliding surface $S_{Qi}(e_{qi},t)$ will be a linear combination of the desired reactive

power error $e_{qi}=Q_{iref}-Q_i$ and its first-order time derivative.

$$S_{Q_i}(e_{Q_i},t) = (Q_{i_{ref}} - Q_i) + K_{Q_i}\frac{d}{dt}(Q_{i_{ref}} - Q_i),$$

The time derivative can be approximated by a discrete time difference, as K_{Qi} has been chosen to obtain a suitable switching frequency, since as stated before, this sliding surface needs to be quantized only in two levels (-1 and+1) using one hysteresis comparator. To fulfill a stability condition similar to considering the input filter dynamics is obtained.

IV.IMPLEMENTATION OF THE DPC-MC AS UPFC

As shown in the block diagram (Fig. 6), the control of the instantaneous active and reactive powers requires the measurement of G_S voltages and output currents necessary to calculate $S_\alpha(e_p,t)$ and $S_\beta(e_Q,t)$ sliding surfaces. The output currents measurement is also used to determine the location of the input currents q component. The control of the matrix converter input reactive power requires the input currents measurement to calculate $S_{Qi}(e_{Qi},t)$. At each time instant, the most suitable matrix vector is chosen upon the discrete values of the sliding surfaces, using tables derived from Tables I and II for all voltage sectors. These vectors do not produce significant effects on the line active and reactive power values, but the lowest amplitude voltage vectors have a high influence on the control of matrix reactive power.

A. Voltage Control in d-q Reference Frame

The output voltages are measured across the capacitors in the output filter and are then feedback separately to the system control. In the d-q reference frame the three- phase output voltages are transformed into two dc signals on the d and q axis.
Using the designed tracking controller on each of the two axes, the presence of the interpreter will ensure a small steady state error on the voltage loop. The control signal in d-q frame are converted back to the ABC reference frame an applied to the modulator. These signal are the reference signal required by the modulator in order to produce the pulses needed to commutate the bi-directional switches. Figure 7 shows the control strategy in d-q reference frame.

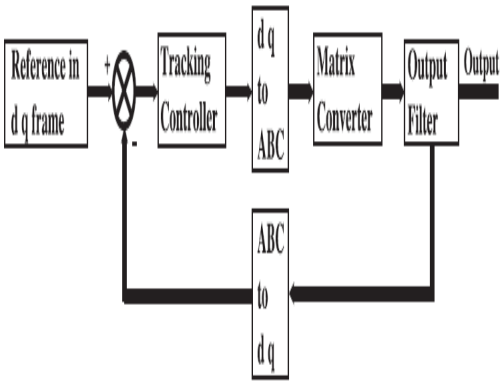


Figure 7: Control strategy in d-q reference frame.

B. Voltage Control in ABC Reference Frame

The problem presented in previous section when the Matrix Converter is connected to an unbalanced load can be solved using a control system working directly in the ABC reference frame. The reference signals which are a set of a three-phase rms voltages at 400Hz in the ABC frame are compared to the voltages measured across the output filter capacitors. The error signal obtained is then applied to the tracking controller on each phase. Each tracking controller generates a control signal which is applied directly to the modulator. Then the modulator produces the pulses required to commutate the bi-directional switches. The general scheme of the system used is shown in Figure 8. The procedure used to design the tracking controller of for the ABC reference is the same as the one used in the design of the tracking controller in the d-q reference frame. In this case because the gain is now set as 0.6. Since the reference of our control is a 400Hz three-phase signal, the interpreter present in the controller will not be able to achieve a small steady state error, being the all closed-loop system of a limited bandwidth. Therefore a gain has been introduced in order to compensate for the amplitude mismatch in the output. The value of this gain has been found to be 6 by trial and error. When the control system was design, the block representing the Matrix Converter was considered as a unity gain. In the practical implementation, the Matrix Converter consists of electronic components which have voltage drops and dissipate energy and therefore the Matrix Converter has a transfer function different from a unity gain. This modifies the closed loop considered in the design of the tracking controller. In the design of the controller, only the output filter has been considered as the plant. The Matrix Converter block is not considered as part of the closed loop. In practice, it have been found that the Matrix Converter can be replaced by a gain with a value between 5 and 6. Also, the block representing the Matrix Converter

introduces a delay. This delay can be compensated by the controller.

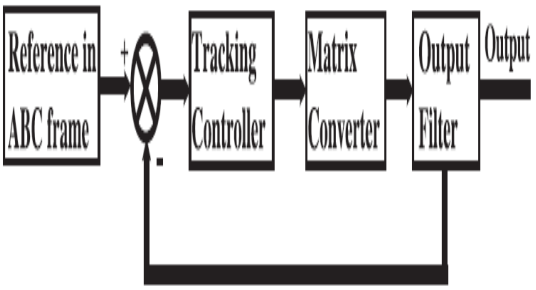


Figure 8: Control strategy in ABC reference frame.

TABLE I
STATE-SPACE VECTORS SELECTION, FOR INPUT VOLTAGES LOCATED AT SECTOR V_i 1

C_α	C_β	Sector $I_0 12 ; I_0 1$ C_{Qi}		$I_0 2 ; I_0 3$ C_{Qi}		$I_0 4 ; I_0 5$ C_{Qi}		$I_0 6 ; I_0 7$ C_{Qi}		$I_0 8 ; I_0 9$ C_{Qi}		$I_0 10; I_0 11$ C_{Qi}	
		+1	-1	+1	-1	+1	-1	+1	-1	+1	-1	+1	-1
-1	+1	-9	+7	-9	+7	-9	+7	+7	-9	+7	-9	+7	-9
-1	0	+3	-1	+3	-1	-1	+3	-1	+3	-1	+3	+3	-1
-1	-1	-6	+4	+4	-6	+4	-6	+4	-6	-6	+4	-6	+4
0	+1	-9	+7	-9	+7	-9	+7	+7	-9	+7	-9	+7	-9
0	0	-2	+2	+8	-8	-5	+5	+2	-2	-8	+8	+5	-5
0	-1	-7	+9	-7	+9	-7	+9	+9	-7	+9	-7	+9	-7
+1	+1	-4	+6	+6	-4	+6	-4	+6	-4	-4	+6	-4	+6
+1	0	+1	-3	+1	-3	-3	+1	-3	+1	-3	+1	+1	-3
+1	-1	-7	+9	-7	+9	-7	+9	+9	-7	+9	-7	+9	-7

TABLE II
STATE-SPACE VECTORS SELECTION FOR DIFFERENT ERROR COMBINATIONS

C_α	C_β	Sector $V_i 12; 1$	$V_i 2; 3$	$V_i 4; 5$	$V_i 6; 7$	$V_i 8; 9$	$V_i 10; 11$
-1	+1	-9; +7	-9; +8	+8; -7	-7; +9	+9; -8	-8; +7
-1	0	+3; -1	+3; -2	-2; +1	+1; -3	-3; +2	+2; -1
-1	-1	-6; +4	-6; +5	+5; -4	-4; +6	+6; -5	-5; +4
0	+1	-9; +7; +6; -4	-9; +8; +6; -5	+8; -7; -5; +4	-7; +9; +4; -6	+9; -8; -6; +5	-8; +7; +5; -4
0	0	Za; Zb; Zc; -8;+2;-5;+8;-2;+5	Za; Zb; Zc; -7;+1;-4; +7;-1;+4	Za; Zb; Zc; +9;-3;+6;-9;+3;-6	Za; Zb; Zc; -8;+2;-5;+8;-2;+5	Za; Zb; Zc; -7;+1;-4; +7;-1;+4	Za; Zb; Zc; -9;+3;-6; +9;-3;+6
0	-1	-6; +4; +9; -7	+5; -6; -8; +9	+5; -4; -8; +7	-4; +6; +7; -9	+6; -5; -9; +8	-5; +4; +8; -7
+1	+1	+6; -4	+6; -5	-5; +4	+4; -6	-6; +5	+5; -4
+1	0	-3; +1	+2; -3	-1; +2	+3; -1	-2; +3	+1; -2
+1	-1	+9; -7	+9; -8	+7; -8	+7; -9	-9; +8	+8; -7

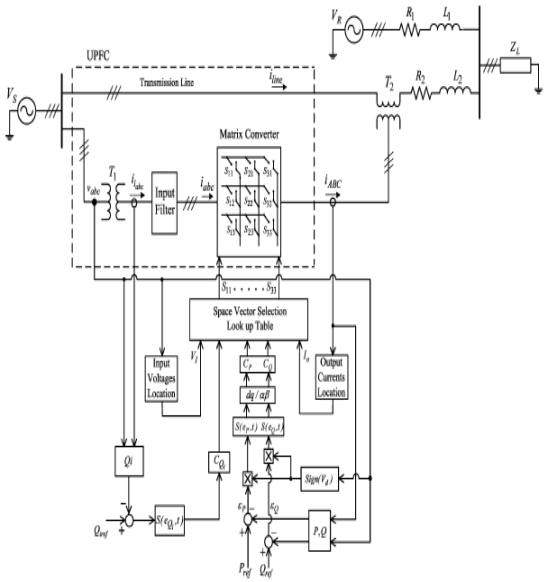
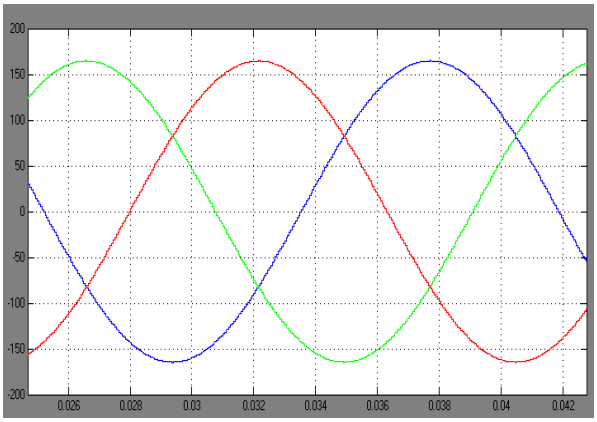


Fig.6. Control scheme of direct power control of the three-phase matrix converter operating as a UPFC.

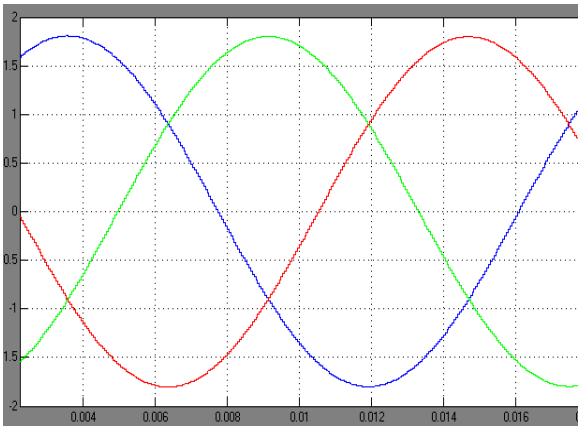
V. SIMULATION RESULTS

The performance of the proposed direct control system was evaluated with a detailed simulation model using the MATLAB/Simulink SimPowerSystems to represent the matrix converter, transformers, sources and transmission lines, and Simulink blocks to simulate the control system. Ideal switches were considered to simulate matrix converter semiconductors minimizing simulation times.

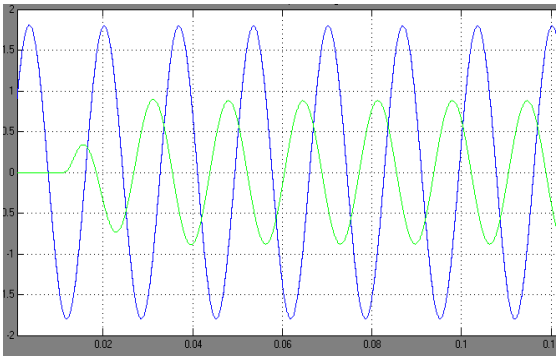
Input voltage:-



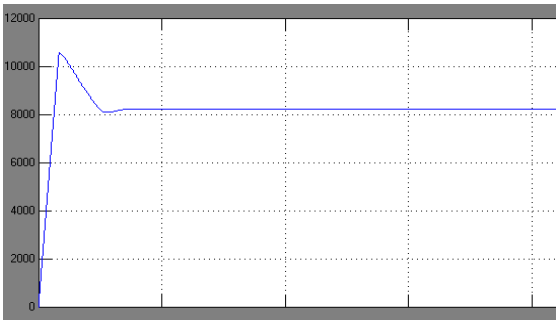
Input current:-



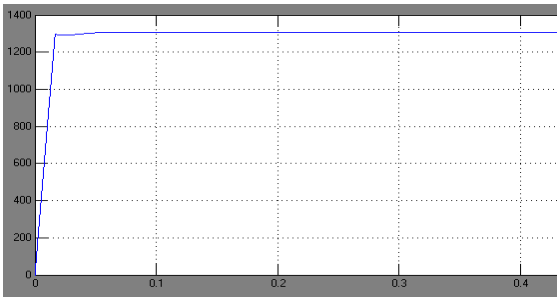
Injected voltage and current:-



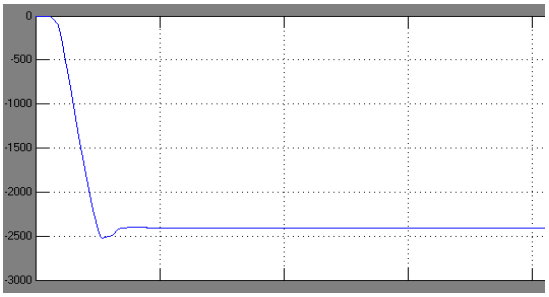
Line active power:-



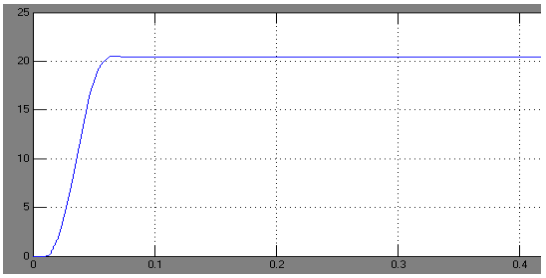
Line reactive power:-



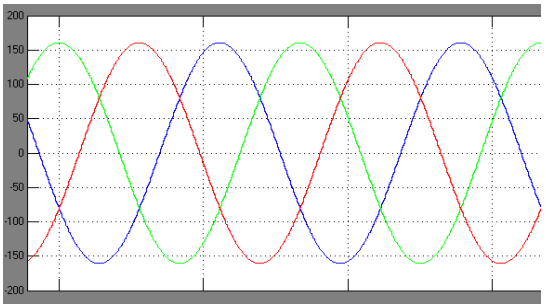
Injected line reactive power:-



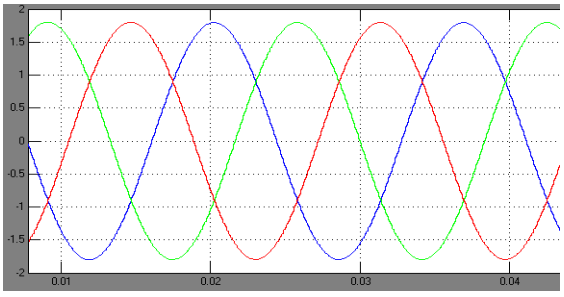
Injected line active power:-



Output voltage:-



Output current:-



VI. CONCLUSION

This paper derived advanced nonlinear direct power controllers, based on sliding mode control techniques, for matrix converters connected to power transmission lines as UPFCs. Presented simulation results show that active and reactive power flow can be advantageously controlled by using the proposed DPC. Results show no steady-state errors, no cross-coupling, insensitivity to nonmodeled dynamics and fast response times, thus confirming the expected performance of the presented

nonlinear DPC methodology. The obtained DPC-MC results were compared to PI linear active and reactive power controllers using a modified Venturini high-frequency PWM modulator. Despite showing a suitable dynamic response, the PI performance is inferior when compared to DPC. Furthermore, the PI controllers and modulator take longer times to compute. Obtained results show that DPC is a strong nonlinear control candidate for line active and reactive power flow. It ensures transmission-line power control as well as sending end reactive power or power factor control.

REFERENCES

[1]. School of Electrical and Electronic Engineering University Park Nottingham, NG72RD" Matrix Converters: A Technology Review" IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 49, NO. 2, APRIL 2002

[2]. Fang Gao, Student Member, and M. Reza Iravani, Fellow, "Dynamic Model of a Space Vector Modulated Matrix Converter" IEEE TRANSACTIONS ON POWER DELIVERY, VOL. 22, NO. 3, JULY 2007

[3]. C Watthanasam, L Zhang, D T W Liang "Analysis and DSP-based Implementation of a Modulation Algorithms for AC-AC Matrix Converters "Dept. of Electronic and, Electrical Engineering University of Bradford, Bradford, BD7 lDP, UK

[4]. Carlos Ortega1, Antoni Arias, Xavier del Toro3, Emiliano Aldabas,Josep Balcells,"Novel Direct Torque Control for Induction Motors using short voltage vectors of Matrix Converters." MIEEE, 1, 2,3,4,5 Technical University of Catalonia.Electronics Engineering Dept. Colom 1, Terrassa 08222, Catalonia, Spain.

[5]. Hong-Hee Lee, Hoang M. Nguyen, Eui-Heon Jung," A Study on Reduction of Common-Mode Voltage in Matrix Converter with Unity Input Power Factor and Sinusoidal Input/Output Waveforms." School of Electrical Engineering University of Ulsan Muger2Dong Nam-gu, Ulsan city Republic of Korea.

[6]. Fan Yue, Patrick W. Wheeler, and Jon C. Clare,"Relationship of Modulation Schemes for Matrix Converters" School of Electrical & Electronic Engineering University of Nottingham, University Park Nottingham, NG7 2RD UK.

K.Meenendranath Reddy was born in Nandyal, A.P, India. He received the B.Tech (Electrical and Electronics Engineering) degree from the madina engineering college, kadapa in 2010: and Pursuing M.Tech (Electrical Power Systems) from the Annamacharya Institute of Technology and Science , rajampeta.
e-mail: kaipa.meenendranathreddy@gmail.com

O.Hemakesavulu was born in Kadapa, A.P, India. He received M.Tech (Power Electronics) degree from Rajeev Gadhi Memorial College of Engineering & Technology, Nandyal And BTech (Electrical and Electronics Engineering) from Annamacharya Institute of Technology and Sciences,Rajampet.Presently pursuing Ph.D. e-mail: hkesavulu 6@gmail.com

M. Padma Lalitha. is awarded Ph.D for her work "Soft Computing Techniques for optimal DG placement in Radial Distribution System " from S.V.U. in the year 2011and is a graduate from JNTU, Anathapur in Electrical & Electronics Engineering in the year 1994. Obtained Post graduate degree in PSOC from S.V.U, Tirupathi in the year 2002. Having 14 years of experience in teaching in graduate and post graduate level. Presently working as Professor and HOD of EEE department in AITS, Rajampet
e-mail: padmalaitha_mareddy @yahoo.co.in

◈◈◈

SUBSTATION MONITORING AND CONTROL USING GSM TECHNOLOGY

[1]V. BHASKAR & [2]T. GOWRI MANOHAR

[1]Department of E.E.E., Srikalahasteeswara Institute of Technology, Srikalahasti, A.P., India,
[2]Department of E.E.E., S.V. University, Tirupati, A.P., India.

Abstract: The purpose of this project is to acquire the remote electrical parameters like Voltage, Current and Frequency and send these real time values over GSM network using GSM Modem/phone along with temperature at power station. This project is also designed to protect the electrical circuitry by operating an Electromagnetic Relay. This Relay gets activated whenever the electrical parameters exceed the predefined values. The Relay can be used to operate a Circuit Breaker to switch off the main electrical supply. User can send commands in the form of SMS messages to read the remote electrical parameter. This system also can automatically send the real time electrical parameters periodically (based on time settings) in the form of SMS. This system can be designed to send SMS alerts whenever the Circuit Breaker trips or whenever the Voltage or Current exceeds the predefined limits. This project makes use of an onboard computer which is commonly termed as microcontroller. This onboard computer can efficiently communicate with the different sensors being used. The controller is provided with some internal memory to hold the code. This memory is used to dump some set of assembly instructions into the controller. And the functioning of the controller is dependent on these assembly instructions. The controller is programmed using Embedded C language.

Keyword: *GSM Modem, Key words - Short Message Service (SMS), Global Systems for Mobile Communication (GSM), AT Command, GSM Modem, relay, circuit breaker (C.B)*

I. INTRODUCTION

Electricity is an extremely handy and useful form of energy. It plays an ever growing role in our modern industrialized society. The electrical power systems are highly non-linear, extremely huge and complex networks. Such electric power systems are unified for economical benefits, increased reliability and operational advantages. They are one of the most significant elements of both national and global infrastructure, and when these systems collapse it leads to major direct and indirect impacts on the economy and national security. A power system consists of components such as generators, lines, transformers, loads, switches and compensators. However, a widely dispersed power sources
And loads are the general configuration of modern power systems. Electric power systems can be divided into two sub-systems, namely, transmission systems and distribution systems. The main process of a transmission system is to transfer electric power from electric generators to customer area, whereas a distribution system provides an ultimate link between high voltage transmission systems and consumer services. In other words, the power is distributed to different customers from the distribution system through feeders, distributors and service mains. Supplying electricity to consumers necessitates power generation, transmission, and distribution. Initially electric power is generated by using electric generators such as: nuclear power generators, thermal power generators and hydraulic power generators and then transmitted through transmission systems using high voltage. Power departs from the generator and enters into a transmission substation, where huge transformers convert the generator's voltage to extremely high voltages (155kV to 765 kV) for long-distance (up to about 300 miles) transmission. Then, the voltage level is reduced using transformers and power is transferred to customers through electric power distribution systems. Power starts from the transmission grid at distribution substations where the voltage is stepped-down (typically to less than 10kV) and carried by smaller distribution lines to supply commercial, residential, and industrial users. Novel electric power systems encompassing of power transmission and distribution grids consist of copious number of distributed, autonomously managed, capital-intensive assets. Such assets comprise: 1.) power plants, 2.) transmission lines, 3.) transformers, and 4.) protection equipment.

Electric utility substations are used in both the transmission and distribution system and operate independently to generate the electricity. A typical substation facility consists of a small building with a fenced-in yard that contains transformers, switches, voltage regulators, and metering equipment that are used to adjust voltages and monitor circuits. A reliable and efficient process of these networks alone is not very significant when these electricity systems are pressed to their parameters of its performance, but also under regular operating conditions. Generators and loads are some components that coerce the continuous dynamic behaviour. The distance between the Generators and loads may be in terms of hundreds of miles. Hence, the amount of huge power exchanges over long distances has turned out as a result of the lack of quality of the electric power. During the earlier development stages the issues on

quality of power were not frequently reported. Quality of supply is a mixture of both voltage quality and the non-technical features of the interaction from the power network to its customers. Demanding the quantity of power being delivered at the user side has raised the alarm due to the increase in demand of electricity in the customer's side. The power generated at the main stations is transported hundreds of miles using transmission lines before they reach the substations. A huge amount of power is lost during the transportation of the generated power which leads to the reduction in the quantity of power received at the substations. Also the electric lines users have identified that the number of drawbacks caused by electrical power quality variations are increasing rapidly.

These variations have already existed on electrical systems, but recently they are causing serious problems. Therefore, measurements must be acquired either from one end or from both the ends of a faulted line. Only meager recorded data is available at limited substation locations in certain systems.

When a fault occurs in such systems, only a few (two or three) recording devices are triggered. The most likely case is that the measurements could not be obtained at either or both ends of the faulted transmission line leads to drop in the quality of the power.

To improve the quality of power with sufficient solutions, it is necessary to be familiar with what sort of constraint has occurred. Additionally, if there is any inadequacy in the protection, monitoring and control of a power system, the system might become unstable. Therefore, it necessitates a monitoring system that is able to automatically detect, monitor, typify and classify the existing constraints on electrical lines. This brings up advantages to both end users and utility companies.

II SYSTEMS COMMUNICATION ARCHITECTURE

As shown in Figure 1 the wireless transference of Monitoring and Control using GSM Technology in this paper is built on the SMS of the GSM network. Data messages produced at one end of the monitoring system are encapsulated into a short message by the gateway and sent to remote monitoring devices at another end. When a short message is received, it can be restored to its original industrial form by removing the SMS PDU head.

This is also conducted by the gateway of the monitoring system. If needed, the message content can be put into other form and forwarded by the gateway through other industrial net work.

Since the transference is a trans-network task, gateways are required to perform protocol conversion along with other functions. The system makes use of the routing function of the GSM network to deliver a message to another gateway. This is not only controlling and also monitoring 33kv/11kv either step-up or step- down substation.

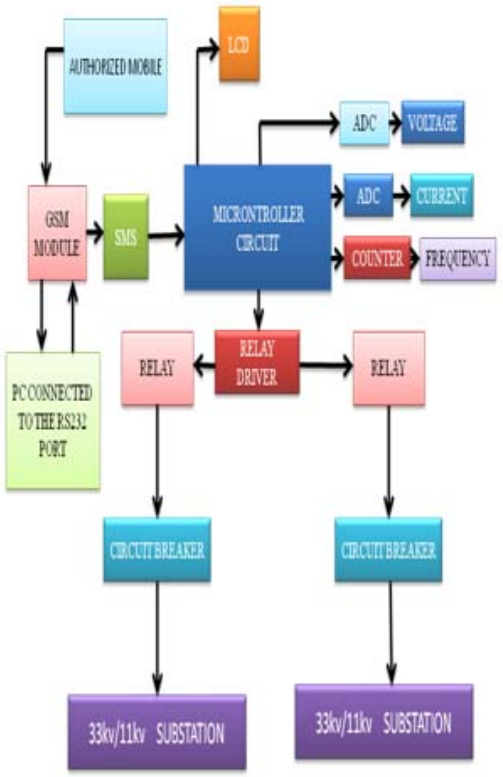


Fig. 1: System Communication Architecture

III. WORKI NG

In this project we are using the GSM technology. A micro controller (also micro controller u nit, MCU or µC) is a small computer on a single integrated circuit consisting of a relatively simple CPU combined with support functions such as a crystal oscillator, timers and etc. Microcontrollers are used in automatically controlled products and devices such a s automobile engine control systems, remote controls, office machines, appliances, power tools and toys. The LCD will give the professional look for the project. It also displays the current operation of the system. The micro controller is used to control the relay drivers depending upon the soft ware program. Major role of this project is to receive the SMS to relay and send the signal to circuit breaker in a substation Initially the SMS is received from the person authorized to use this setup (destination) by the GSM modem (SIM300 MODEM) & is transferred to the microcontroller r devices kit with the help of a MAX 232 chip. As per the AT commands given by the microcontroller to the modem, the control signal from

the SMS is extracted and is used to control the devices connected to it. We have to convert the 'septets' of the to phone to 'octets' because the micro-controller need bytes with 8 bits length (The 'septet' is 1 byte with 7 bits length and 'octet' is 1 byte with 8 b its length). All this process is necessary t o decode the message from SMS.

A program (for extracting the control signal part from received SMS) is loaded into microcontroller devices kit, and then the circuit is connected to the modem. The microcontroller now tries to read the SMS from t he 1st memory location of the modem and it keeps trying again until the modem receives any (programmed for every one second). Before implementing the control signal part of t he SMS, the modem extracts the number from the SM S and verifies if this number has the access to control the device or not. For controlling the device s, the message will be sent in hexa decimal format. The hex data is converted to the equivalent binary and the particular output is enabled. For example if the message is "**AB**" the equivalent binary is "10101011" this implies that the output 1, 3, 5, 7, 8 are enabled and the remaining ports are disabled. We have connected LEDs to the ports of micro controller to show the output and their status indicates whether the ports are set to 'ON' or 'OFF'. And substation control and monitoring like send the message in text format like SUBSTATION 1ON and SUBSTATION 2ON and SUBSTATION 1OFF and SUBSTATION 2OFF.

IV. COMPONENTS USED

Power Supply: 5v and 3.6v and 4.6v, 12v DC
Micro controller: Philips P89V51RD2-8bit.
LCD: 16x2 characters
RS 232 converter: MAX 232 Flash Magic: Vision 2.4
Keil-C m-vision: µVision3 (IDE -Version)

V . GSM COMMANDS

Commands always start with AT (which means Attention) and finish with a <CR> character. Information responses and result codes, Responses start and end with <CR><LF>, except for the ATV0 DCE response format) and the ATQ1 (result code suppression) commands.
If command syntax is incorrect, an ERROR string is returned.
If command syntax is correct but with some incorrect parameters, the +CME ERROR:
<Err> or +CMS ERROR: <sms Err> strings are returned with different error codes.
If the command line has been performed successfully, an OK string is returned.
In some cases, such as "AT+CPIN?" or (unsolicited) incoming events, the product does not return the OK string as a response.

In the following examples <CR> and <CR><LF> are intentionally omitted.
1. Manufacturer identification +CGMI
2. Request model identification +CGMM
3. Request revision identification +CGMR
4. Product Serial Number +CGSN
Preferred Message Format +CMGF
Description: The message formats supported are text mode and PDU mode. In PDU mode, a complete SMS Message including all header information is given as a binary string (in hexadecimal format).Therefore, only the following set of characters is allowed:

{„0□,□1□,□2□,□3□,□4□,□5□,□6□,□7□,□8□, □9□,„A□,„B□,□C□,□D□,□E□,□F□}. Each pair or characters are converted to a byte (e.g.: „41□ is converted to the ASCII character „A□, whose ASCII code is 0x41 or 65). In Text mode, all commands and responses are in ASCII characters. The format selected is stored in EEPROM by the +CSAS command.
Command syntax: AT+CMGF
Read message +CMGR
Description: This command allows the application to read stored messages. The messages are read from the memory selected by +CPMS command.
Command syntax: AT+CMGR=<index>
Send message +CMGS
Description: The <address> field is the address of the terminal to which the message is sent. To send the message, simply type, <ctrl-Z> character (ASCII 26). The text can contain all existing characters except <ctrl-Z> and <ESC>(ASCII 27).This command can be aborted using the <ESC> character when entering text. In PDU mode, on hexadecimal characters are used
(„0□…□9□, □A□…□F□).
Syntax: AT+CMGS= <length> <CR>
PDU is entered <ctrl-Z / ESC >.

VI .MICROCONTROLLER

Description: The 89C51RB2/RC2/RD2 device contains a non-volatile 16kB/32kB/64kB Flash program memory that is both parallel programmable and serial In-System and In-Application Programmable.

In-System Programming (ISP) allows the user to download new code while the microcontroller sits in the application. In-Application Programming (IAP) means that the microcontroller fetches new program code and reprograms itself while in the system. This allows for remote programming over a modem link. A default serial loader (boot loader) program in ROM allows serial In-System programming of the Flash memory via the UART without the need for a loader in the Flash code. For In Application Programming, the user program erases and reprograms the Flash

memory by use of standard routines contained in ROM. This device executes one machine cycle in 6 clock cycles, hence providing twice the speed of a conventional 80C51.

This device is a Single-Chip 8-Bit Microcontroller manufactured in advanced CMOS process and is a derivative of the 80C51 microcontroller family. The device also has four 8-bit I/O ports, three 16-bit timer/event counters, a multi-source, and four-priority-level, nested interrupt structure, an enhanced UART and on-chip oscillator and timing circuits.

The added feature of the P89C51RB2/RC2/RD2 makes it a powerful microcontroller for applications that require pulse width modulation, high-speed I/O and up/down counting capabilities such as motor control.

VII . A DEVELOPMENT TOOLS

Keil (µVision 2): The Keil C51 Cross Compiler is an ANSI C Compiler that is written specifically to generate fast, compact code for the 8051 microcontroller family. The C51 Compiler generates object code that matches the efficiency and speed of assembly programming. Using a high-level language like C has many advantages over assembly language *programming:*

- Knowledge of the processor instruction set is not required. Rudimentary knowledge of the memory structure of the 8051 CPU is desirable (but not necessary).
- Details like register allocation and addressing of the various memory types and data types is managed by the compiler.
- Programs get a formal structure (which is imposed by the C programming language) and can be divided into separate functions. This contributes to source code reusability as well as better overall application structure.
- The ability to combine variable selection with specific operations improves program readability.
- Keywords and operational functions that more nearly resemble the human thought process may be used.
- Programming and program test time is drastically reduced.
- The C run-time library contains many standard routines such as: formatted output, numeric conversions, and floating-point arithmetic.
- Existing program parts can be more easily included into new programs because of modular program construction techniques.
- The language C is a very portable language (based on the ANSI standard) that enjoys wide popular support and is easily obtained for most systems.

VIII . FLOW CHART AND SOFTWARE IMPLEMENTATION

Software development: The software for the system is developed in Embedded C and Visual Basic. The flowcharts depicting the monitoring and control the different voltage level of substations and also control the circuit breaker is shown in fig2.

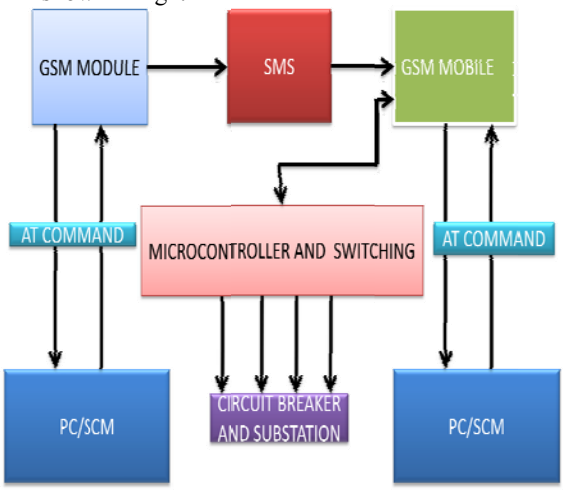
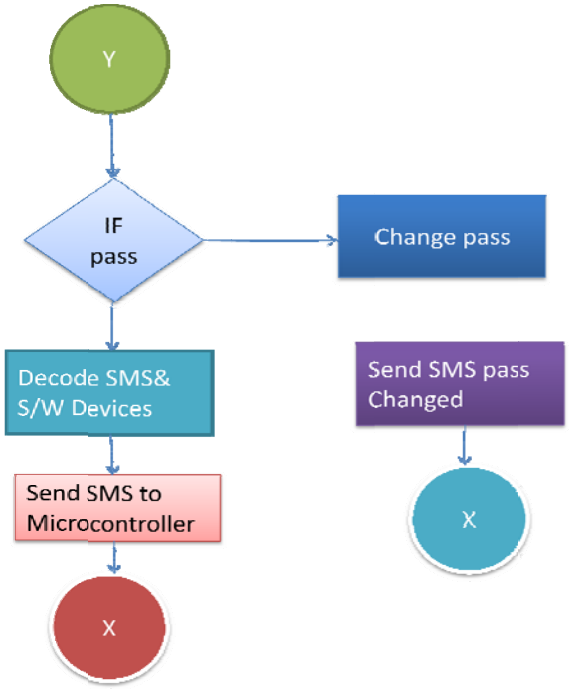
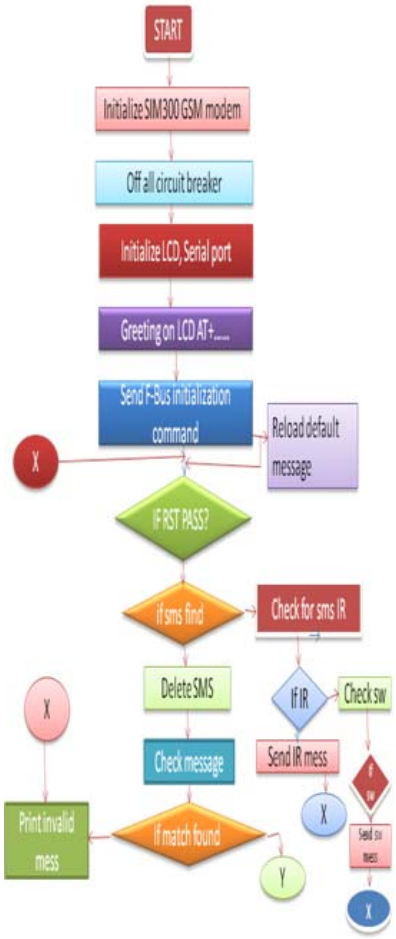


Fig. 8: Software Implementation

IX .FLOW CHART





X . CONCLUSION

The project "SUBSTATION MONITORING AND CONTROL USING GSM TECHNOLOGY" was designed such that the devices can be monitored and also controlled from anywhere in the world using GSM modem connected to mobile phone Integrating features of all the hardware components used have been developed in it. Presence of every module has been reasoned out and placed carefully, thus contributing to the best working of the unit. Secondly, using highly advanced IC□s with the help of growing technology, the project has been successfully implemented. Thus the project has been successfully designed and tested.

REFERENCES:

[1]. Jyotishman Pathak, Yuan Li, Vasant Honavar and James D. McCalley, "A Service-Oriented Architecture for Electric Power Transmission System Asset Management", In ICSOC Workshops, pp: 26-37, 2006.

[2]. B. A. Carreras, V. E. Lynch, D. E. Newman and I. Dobson, "Blackout Mitigation Assessment in Power Transmission Systems", Hawaii International Conference on System Science, January 2003.

[3]. Xiaomeng Li and Ganesh K. Venayagamoorthy, "A Neural Network Based Wide Area Monitor for a Power System", *IEEE Power Engineering Society General Meeting*, Vol. 2, pp: 1455-1460, 2005.

[4]. Argonne National Laboratory, "Assessment of the Potential Costs and Energy Impacts of Spill Prevention, Control, and Countermeasure equirements for Electric Utility Substations", Draft Energy Impact Issue Paper, 2006.

[5]. Gsm based Motor monitoring and speed control by V.Bhaskar International Journal of Mechanical and Industrial Engineering (IJMIE), ISSN No. 2231 –6477, Volume-1, Issue-2, 2011

[6]. Daponte, M. Di Penta and G.Mercurio, "TRANSIENTMETER: A Distributed Measurement System for Power Quality Monitoring", *IEEE Transactions on Power Delivery*, Vol. 19, Issue. 2, pp: 456-463, 2004.

[7]. G. Pudlo, S. Tenbohlen, M. Linders and G. Krost, "Integration of Power Transformer Monitoring and Overload Calculation into the Power System Control Surface", *IEEE/PES Transmission and Distribution Conference and Exhibition*, Vol. 1, pp: 470-474 Asia Pacific, 2002.

[8]. Zhi-Hua Zhou, Yuan Jiang, Xu-Ri Yin, and Shi-Fu Chen, "The Application of Visualization and Neural Network Techniques in a Power Transformer Condition Monitoring System", In: T. Hendtlass and M. Ali eds. Lecture Notes in Artificial Intelligence 2358, Berlin: Springer- Verlag, pp: 325-334, 2002.

◈◈◈

AN FPGA IMPLEMENTATION OF MODIFIED DECISION BASED UNSYMMETRICAL TRIMMED MEDIAN FILTER FOR THE REMOVAL OF SALT AND PEPPER NOISE IN DIGITAL IMAGES

CHAITANYA BETHINA & M.PREMKUMAR

Department of Electronics and Communications, Shri Vishnu Engineering College for Women , Bhimavaram, India

Abstract- A modified decision based unsymmetrical trimmed median filter algorithm for the restoration of gray scale, and color images that are highly corrupted by salt and pepper noise is proposed in this paper. Images are often corrupted by impulse noise during acquisition and transmission; thus, an efficient noise suppression technique is required before subsequent image processing operations. Median filter (MF) is widely used in noise removal methods due to its denoising capability and computational efficiency. However, it is effective only for low noise densities. Extensive experimental results demonstrate that our method can obtain better performances in terms of both subjective and objective evaluations than denoising techniques. Especially, the proposed method can preserve edges very well while removing salt and pepper noise. Modified Decision Based Algorithm (MDBA), and Progressive Switched Median Filter (PSMF) shows better results at low and medium noise densities. At high noise densities, their performance is poor. A new algorithm to remove high-density salt and pepper noise using modified Decision Based Unsymmetric Trimmed Median Filter (DBUTMF) is proposed. The proposed algorithm replaces the noisy pixel by trimmed median. Since our algorithm is algorithmically simple, it is very suitable to be applied to many real-time applications and higher noise densities. When all the pixel values are 0's and 255's then the noise pixel is replaced by mean value of all the elements present in the selected window. The proposed algorithm is tested against different grayscale and color images and it gives better Peak Signal-to-Noise Ratio (PSNR) and Image Enhancement Factor (IEF).

***Index Terms**--Median filter, salt and pepper noise, unsymmetrical trimmed median filter*

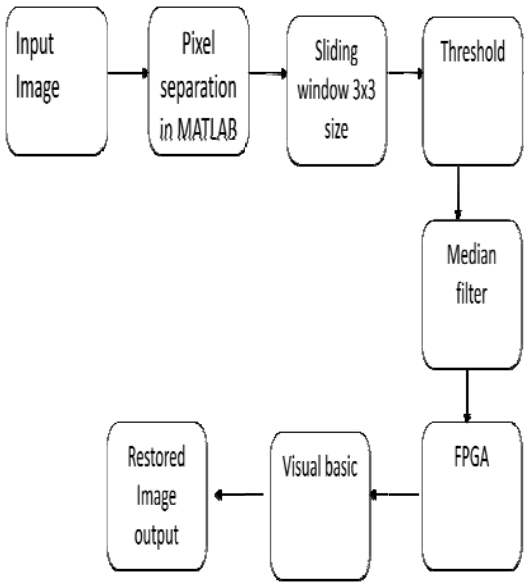
I. INTRODUCTION

Images are often corrupted by salt and pepper noise due to error in transmission of digital images. There are two types of impulse noise, they are salt and pepper noise and random valued noise. Salt and pepper noise can corrupt the images where the corrupted pixel takes either maximum or minimum gray level. The objective of noise removal is to eliminate the salt and pepper noise with minimum deformation caused to the image. The new algorithm has lower computation time when compared to other standard algorithms. Results of the algorithm is compared with various existing algorithms and it is proved that the new method has better visual appearance and quantitative measures at higher noise densities In this standard median filter will be effective only at low noise densities. The standard median (SM) filter is a simple nonlinear smoother that can suppress noise while retaining sharp sustained changes (edges) in signal values. It is particularly effective in reducing impulsive-type noise. In An adaptive median filter (AMF). The nonlinear mean filter cannot remove such positive and negative impulses simultaneously many switched median filters were proposed to detect and correct only the corrupted pixel. But at high noise densities the window size has to be increased which may lead to blurring the image. In switching median filter the major drawback is defining that a robust decision is difficult. Especially when the noise level is high.

× To overcome the above drawback, Decision Based Algorithm (DBA) is proposed. In this, image is denoised by using a 3*3 window. Decision-based median filtering algorithm in which local image structures are used to estimate the original values of the noisy pixels.

In such case, neigh- boring pixel is used for replacement. This repeated replacement of neighboring pixel produces streaking effect. In order to avoid this drawback, Decision Based Unsymmetric Trimmed Median Filter (DBUTMF) is proposed. In case if the selected window contains all the values as 0 s and 255 s

means then trimmed median value cannot be obtained, so this is also not an effective one. Due to these the algorithm does not give better results at very high noise density that is at 80% to 90.Due to this the proposed Modified Decision Based Un- symmetric Trimmed Median Filter (MDBUTMF) algorithm re- moves this drawback at high noise density and gives better Peak Signal-to-Noise Ratio (PSNR) and Image Enhancement Factor (IEF) values than the existing algorithm.



The above block diagram mainly consists of taking at 256/256 image and adding noise to it and converting a noise image into a matrix and then dividing a entire matrix into 3×3 siding window, after dividing that window the sliding window is applied with our MDBUTMF to eliminate the noise pixel. This is represented as 0 and 255 after the eliminating noise pixel by images convert into text format. The text format is converted into bit stream. which is compatible to a FPGA kit is used by Spartan 3E which consist of micro blaze processor which is 32 bit processor consisting of RISC(Reduced Instruction Set) architecture. The output of FPGA kit is visualized in visual basic where the noise less image is retrieved.

A brief introduction of unsymmertric trimmed median filter is given in Section II. Section III describes about the proposed algorithm and different cases of proposed algorithm. The detailed description of the proposed algorithm with an example is presented in Section IV. Simulation results with different images are presented in Section V. Finally conclusions are drawn in Section VI.

II. UNSYMMETRIC TRIMMED MEDIAN FILTER

The idea behind a trimmed filter is to reject the noisy pixel from the selected 3*3 window. Alpha Trimmed Mean Filtering (ATMF) is a symmetrical filter where the trimming is symmetric at either end. A fixed impulse noise detector using unsymmetrical trimmed variants for the removal of high density salt and pepper noise for corrupted gray scale image is proposed. The proposed algorithm utilizes an impulse detector based on the threshold value obtained by unsymmetrical trimmed variants to check, if the pixel is noisy or not. In this median value is used to replace the noisy pixel. This filter is called trimmed median filter because the pixel values 0's and 255's are removed from the selected window. For high noise densities it does not preserve the image information due to the elimination of outlier values. Unsymmetrical trimmed filter replaced the symmetrical counterpart. The trimming was not uniform as in the previous case; So for the removal of salt and pepper noise at high noise densities with edge preservation (MDBUTMF) Modified decision based unsymmetrical trimmed median filter is proposed.

III. PROPOSED ALGORITHM

The proposed Modified Decision Based Unsymmetric Trimmed Median Filter (MDBUTMF) and Salt and Pepper Noise Reduction Method avoid the above drawback even at high noise densities. The proposed method provides better Peak Signal-to-Noise Ratio (PSNR) than the existing methods. The proposed filter (MDBUTMF) replaces the noisy pixel by trimmed median value when some of the elements with values 0 s and 255 s are present in the selected window. If all the pixel values in the selected window are 0 s and 255 s means then the noisy pixel is replaced by mean value of all the elements present in that selected window. The throughput of MDBUTMF is a noise removal image. That is, if the processing pixel lies between maximum and minimum gray level values then it is noise free pixel, it is left unchanged. If the processing pixel takes the maximum or minimum gray level then it is noisy pixel which is processed by MDBUTMF. The steps of the MDBUTMF are elucidated as follows

Step 1*:* Select 2-D window of size 3×3. Assume that the pixel being processed is Pij.

Step 2: If 0 < Pij < 255 then Pij is an uncorrupted pixel and its value is left unchanged. This is illustrated in Case iii) of Section IV.

Step 3**:** If Pij=0 or Pij=255 then Pij is a corrupted pixel then two cases are possible as given in Case i) and ii).

Case i): If the selected window contains all the elements as 0's and 255's. Then replace Pij with the mean of the element of window.

Case ii): If the selected window contains not all elements as 0's and 255's. Then eliminate 255's and 0's and find the median value of the remaining elements. Replace Pij with the median value.

Step 4*:* Repeat steps 1 to 3 until all the pixels in the entire image are processed.

The pictorial representation of each case of the proposed algorithm is shown in Fig. 1. The detailed description of each case of the flow chart shown in Fig. 1 is illustrated through an example in Section IV.

IV. ILLUSTRATION OF MDBUTMF ALGORITHM

Each and every pixel of the image is checked for the presence of salt and pepper noise. Different cases are illustrated in this Section. If the processing pixel is noisy and all other pixel values are either 0's or 255's is illustrated in Case i). If the processing pixel is noisy pixel that is 0 or 255 is illustrated in Case ii). If the processing pixel is not noisy pixel and its value lies between 0 and 255 is illustrated in Case iii).

Case i) if the selected window contains salt/pepper noise as processing pixel (i.e., 255/0 pixel value) and neighboring pixel values contains all pixels that adds salt and pepper noise to the image:

$$\begin{pmatrix} 0 & 255 & 0 \\ 0 & <255> & 0 \\ 255 & 0 & 255 \end{pmatrix}$$

Where "255" is processing pixel, i.e., (Pij).

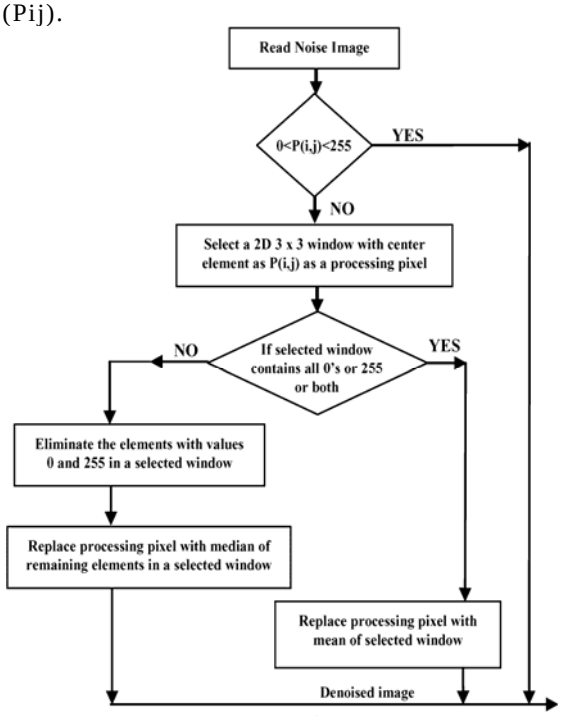


Fig 1. Flow chart of MDBUTMF.

Since all the elements surrounding (Pij) are 0's and 255's. If one takes the median value it will be either 0 or 255 which is again noisy. To solve this problem, the mean of the selected window is found and the processing pixel is replaced by the mean value. Here the mean value is 170. Replace the processing pixel by 170.

Case ii): If the selected window contains salt or pepper noise as processing pixel (i.e., 255/0 pixel value) and neighboring pixel values contains some pixels that adds salt (i.e., 255 pixel value) and pepper noise to the image:

$$\begin{pmatrix} 78 & 90 & 0 \\ 120 & <0> & 255 \\ 97 & 255 & 73 \end{pmatrix}$$

Where "0" is processing pixel, i.e.,(Pij) .

Now eliminate the salt and pepper noise from the selected window. That is, elimination of 0's and 255's. The 1-D array of the above matrix is [78 90 0 120 0 255 97 255 73]. After elimination of 0's and 255's the pixel values in the selected window will be [78 90

120 97 73]. Here the median value is 90. Hence replace the processing pixel Pij by 90.
Case iii): If the selected window contains a noise free pixel as a processing pixel, it does not require further processing. For example, if the processing pixel is 90 then it is noise free pixel:

$$\begin{bmatrix} 43 & 67 & 70 \\ 55 & \langle 90 \rangle & 79 \\ 85 & 81 & 66 \end{bmatrix}$$

Where "90" is processing pixel, i.e.,(Pij).Since "90" is a noise free pixel it does not require further processing.

V. SIMULATION RESULTS

The performance of the proposed algorithm is tested with different gray scale and color images. The noise density (intensity) is varied from 10% to 90%. For implementing our algorithm, we have used MATLAB 7 on a 2.80 GHz Pentium R processor with 1 GB of RAM. The performances of the proposed algorithm are quantitatively measured by the Peak Signal to Noise Ratio (PSNR) and Image Enhancement Factor (IEF as defined in (1) and (3), respectively:

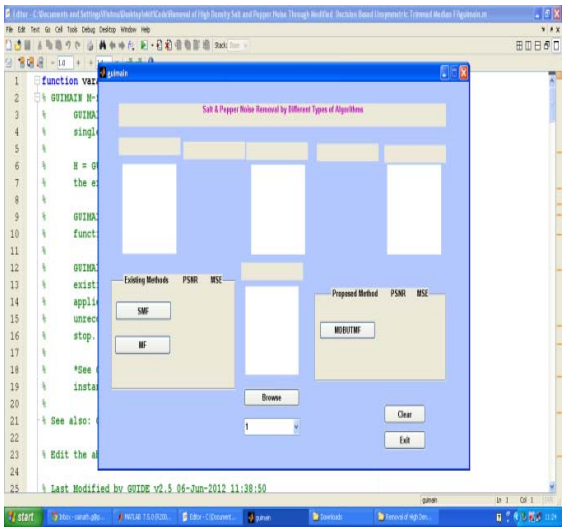


TABLE I
COMPARISON OF PSNR VALUES OF DIFFERENT ALGORITHMS FOR LENA IMAGE AT DIFFERENT NOISE DENSITIES

Noise in %	PSNR in dB					
	MF	AMF	PSMF	DBA	MDBA	MDBUTMF
10	26.34	28.43	30.22	36.4	36.94	37.91
20	25.66	27.40	28.39	32.9	32.69	34.78
30	21.86	26.11	25.52	30.15	30.41	32.29
40	18.21	24.40	22.49	28.49	28.49	30.32
50	15.04	23.36	19.13	26.41	26.52	28.18
60	11.08	20.60	12.10	24.83	24.41	26.43
70	9.93	15.25	9.84	22.64	22.47	24.30
80	8.68	10.31	8.02	20.32	20.44	21.70
90	6.65	7.93	6.57	17.14	17.56	18.40

TABLE II
COMPARISON OF IEF VALUES OF DIFFERENT ALGORITHMS FOR LENA IMAGE AT DIFFERENT NOISE DENSITIES

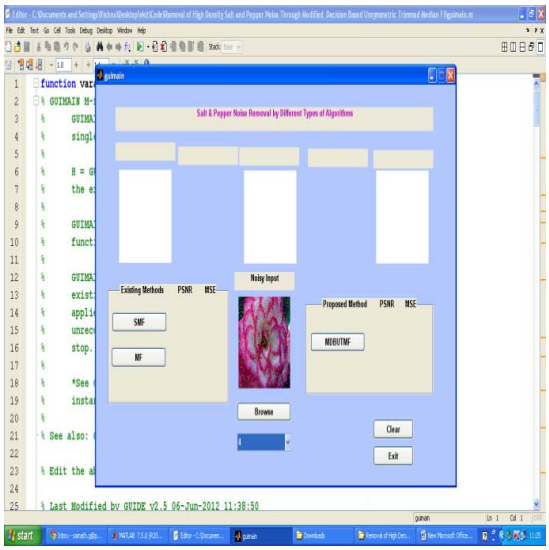
Noise Density	Median Filter	Switching Median Filter	MDBUTMF
1%	42.105	36.579	51.4779
2%	40.1528	36.2234	46.53315
3% 4% 5% MSE	39.2938 38.1312 37.4737	35.7106 35.2816 34.8293	46.1503 43.8922 41.9527
1% 2% 3% 4% 5%	4.0042 6.2776 7.6506 9.06 11.6336	14.2945 15.5146 17.4589 19.2718 21.3872	0.4626 1.4437 1.5779 2.65378 4.14771

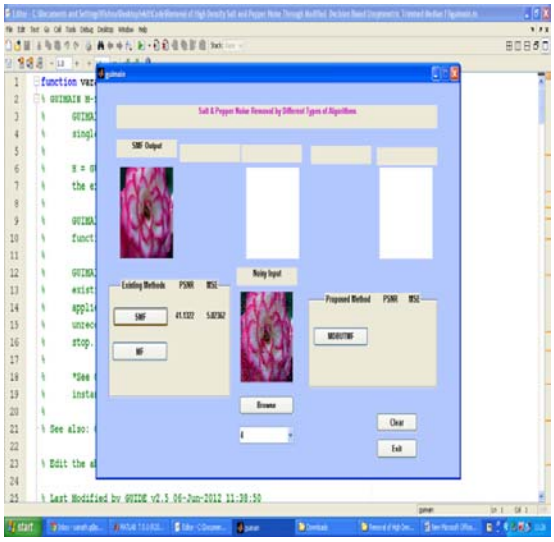
$$\text{PSNR in dB} = 10log10\left(\frac{255^2}{MSE}\right)$$

$$MSE = \sum_i \sum_j (Y(i,j) - \dot{Y}(i.j))^2 / M \times N$$

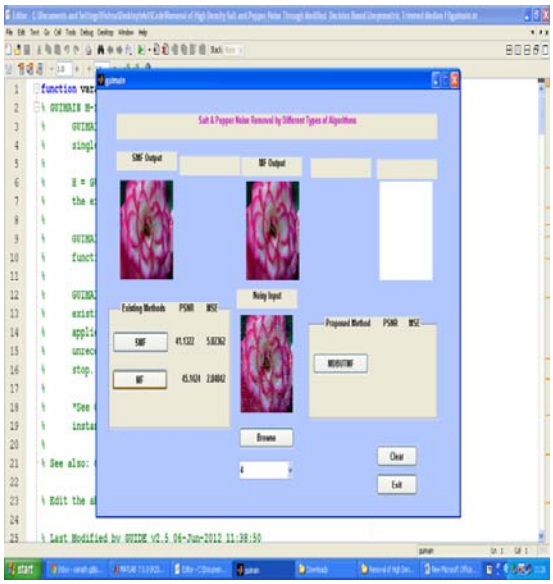
$$IEF = \frac{\sum_i \sum_j (\eta(i,j) - y_{(i,j)})^2}{\sum_i \sum_j (\hat{y}(i,j) - y_{(i,j)})^2}$$

Where MSE stands for mean square error, IEF stands for image enhancement factor, is size of the image, Y represents the original image, denotes the denoised image, and represents the noisy image.

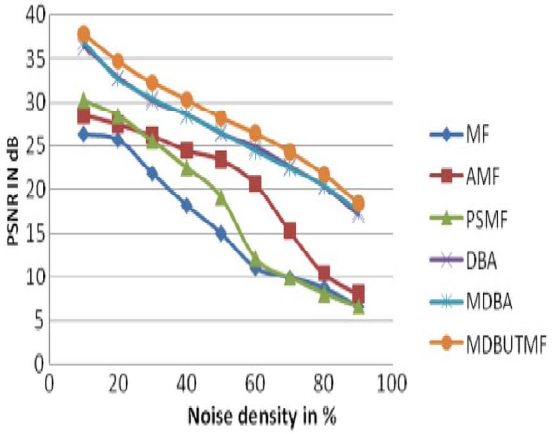




The PSNR and IEF values of the proposed algorithm are compared against the existing algorithms by varying the noise density from 10% to 90% and are shown in Table I and Table II. From the Tables I and II, it is observed that the performance of the proposed algorithm (MDBUTMF) is better than the existing algorithms at both low and high noise densities. A plot of PSNR and IEF against noise densities for Lena image is shown in Fig. 2.



The qualitative analysis of the proposed algorithm against the existing algorithms at different noise densities for Baboon image is shown in Fig. 3. In this figure, the first column represents the processed image using MF at 80% and 90% noise densities. Subsequent columns represent the processed images for AMF, PSMF, DBA, MDBA and MDBUTMF.



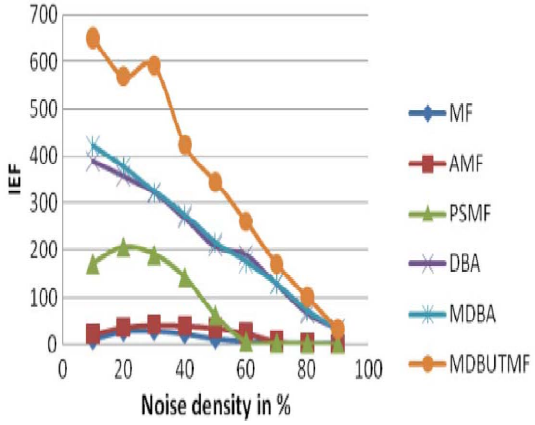
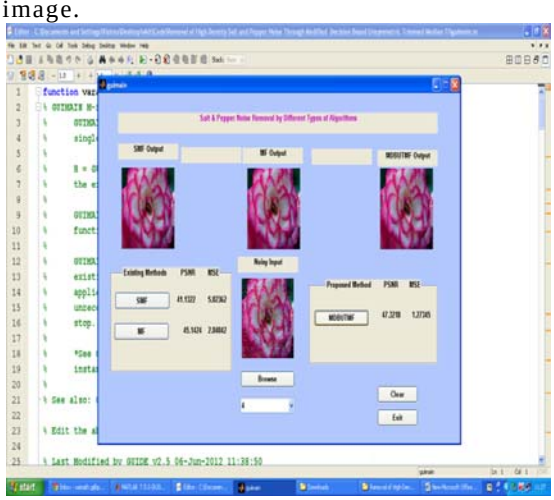


Fig 2. Comparison graph of PSNR and IEF at different noise densities for Lena image.

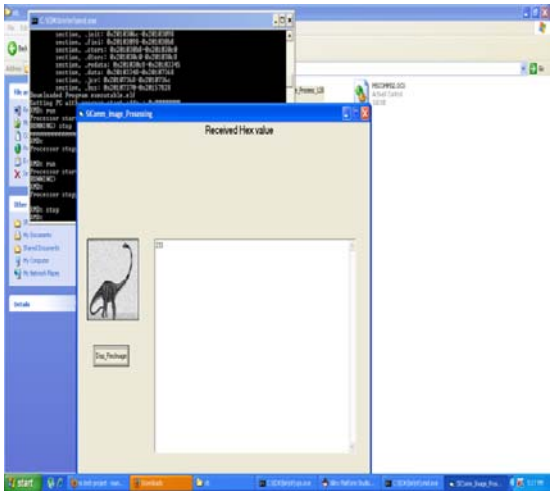
TABLE III
COMPARISON OF PSNR VALUES OF DIFFERENT TEST IMAGES AT NOISE DENSITY OF 70%

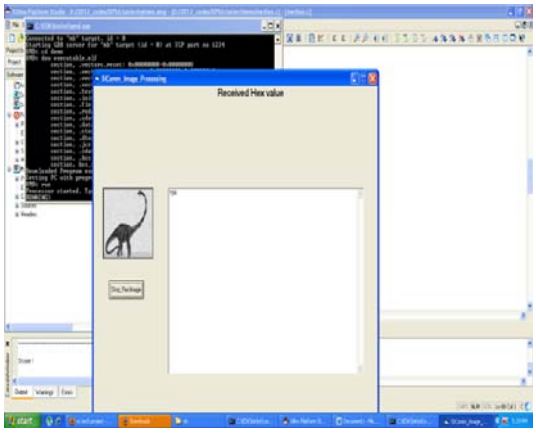
Test images	PSNR in dB					
	MF	AMF	PSMF	DBA	MDBA	MDBUTMF
Camcraman	9.46	13.93	9.47	20.84	19.97	22.52
Lena	9.93	15.25	9.84	22.64	22.47	24.30
Baboon	10.11	14.86	10.05	22.35	20.54	23.80

The proposed algorithm is tested against images namely Cameraman, Baboon and Lena. The images are corrupted by 70% "Salt and Pepper" noise. The PSNR values of these images using different algorithms are given in Table III. From the table, it is clear that the MDBUTMF gives better PSNR values irrespective of the nature of the input image.



The MDBUTMF is also used to process the color images that are corrupted by salt and pepper noise. The color image taken into account is Baboon. In Fig. 4, the first column represents the processed image using MF at 80% and 90% noise densities. it can be observed that the performance of the proposed algorithm is better than the existing algorithms at high noise densities. Not all the elements in a selected 3 x 3 window is 255s or zeros at medium noise density. Hence, the proposed algorithm is almost same PSNR value against MDBUTMF at medium noise density. Subsequent columns represent the processed images for PSMF, DBA, MDBA and MDBUTMF. From the figure, it is possible to observe that the quality of the restored image using proposed algorithm is better than the quality of the restored image using existing algorithms.





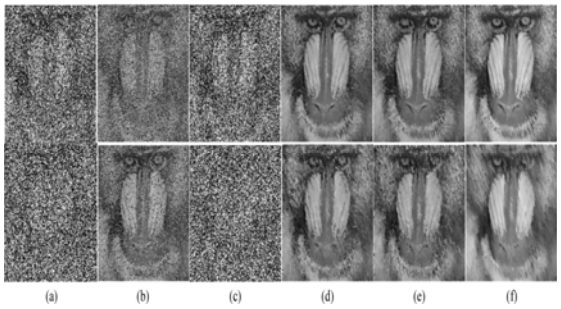


Fig. 3. Results of different algorithms for Baboon image. (a) Output of MF. (b) Output of AMF. (c) Output of PSMF. (d) Output of DBA. (e) Output of MDBA.(f) Output of MDBUTMF. Row 1 and Row 2 show

processed results of various algorithms for image corrupted by 80% and 90% noise densities, respectively.

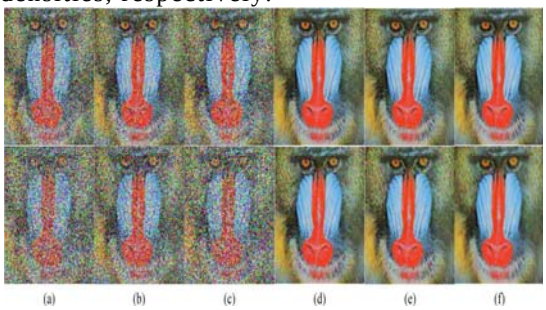


Fig. 4. Results of different algorithms for color Baboon image. (a) Output of MF. (b) Output of AMF. (c) Output of PSMF. (d) Output of DBA. (e) Output of MDBA. (f) Output of MDBUTMF. Rows 1 and 2 show processed results of various algorithms for color image corrupted by 70% and 80% noise densities, respectively.

VI. CONCLUSION

A new algorithm (MDBUTMF) is proposed which gives better performance in comparison with the existing non-linear filter like Standard Median Filter (SMF), Adaptive Median Filter (AMF), Decision Based Algorithm (DBA) Modified Decision Based Algorithm (MDBA), and Progressive Switched Median Filter (PSMF) algorithms. These existing impulse noise removal algorithms are in terms of PSNR and IEF. The performance of the algorithm has been tested at low, medium and high noise densities on both gray-scale and color images. Even at high noise density levels the MDBUTMF gives better results .Both visual and quantitative results are demonstrated and it is also applied to many real-time applications The proposed algorithm is effective for salt and pepper noise removal in images at high noise densities.

REFERENCES

[1] P. E. Ng and K. K. Ma, "A switching median filter with boundary discriminative noise detection for extremely corrupted images," IEEE Trans. Image Process. vol. 15, no. 6, pp. 1506–1516, Jun. 2006.

[2] K. S. Srinivasan and D. Ebenezer, "A new fast and efficient decision based algorithm for removal of high density impulse noise," IEEE Signal Process. Lett., vol. 14, no. 3, pp. 189–192, Mar. 2007.

[3] V. Jayaraj and D. Ebenezer, "A new switching-based median filtering scheme and algorithm for removal of high-density salt and pepper noise in image," EURASIP J. Adv. Signal Process., 2010.

[4] K. Aiswarya, V. Jayaraj, and D. Ebenezer, "A new and efficient algorithm for the removal of high density salt and pepper noise in images and videos," in Second Int. Conf. Computer Modeling and Simulation, 2010, pp. 409–413

◈◈◈

A NOVEL MULTIPHASE BIDIRECTIONAL FLY-BACK CONVERTER TOPOLOGY IS APPLIED TO INDUCTION MOTOR DRIVE

M.RAMA MOHANA RAO & CH.RAMBABU

Department of Electrical and Electronics Engineering,
Sri vasavi engineering college,Tadepalligudem

Abstract- Hybrid Electric Vehicle (HEV) is an emerging technology in the modern world because of the fact that it mitigates environmental pollutions and at the same time increases fuel efficiency of the vehicles. Bi-directional Fly – back Converter controls electric drive of HEV of high power and enhances its performance which is the reflection of the fact that it can generate Constant voltages. For hybrid electric vehicles, the batteries and the drive dc link may be at different voltages. The batteries are at low voltage to obtain higher volumetric efficiencies, and the dc link is at higher voltage to have higher efficiency on the motor side. Therefore, a power interface between the batteries and the drive's dc link is essential. This power interface should handle power flow from battery to motor, motor to battery, external gen-set to battery, and grid to battery. This paper proposes a multi-power-port topology which is capable of handling multiple power sources and still maintains simplicity and features like obtaining high gain, wide load variations, lower output-current ripple, and capability of parallel-battery energy due to the modular structure. The scheme incorporates a transformer winding technique which drastically reduces the leakage inductance of the coupled inductor. The development and testing of a bidirectional fly-back dc–dc converter for hybrid electric vehicle is described in this paper. Simple hysteresis voltage control is used for dc-link voltage regulation. The simulation results are presented, and modeling the circuit by using MATLAB/SIMULINK Platform.

Keywords: *Bidirectional fly-back converter, hybrid electric Vehicle, leakage inductance.*

I. INTRODUCTION

The ever-increasing need for oil combined with a worldwide increasing traffic density, regulatory requirements for reduced emissions, and the ongoing discussion about climate change present strong incentives for the automotive industry to further improve the car drive trains, to reduce fuel consumption, and to lower emissions of exhaust gases that are harmful to the environment, such as carbon dioxide. The required efficiency improvement can be achieved with a hybrid drive train which combines an electric motor and a combustion engine in a way that facilitates the most desirable operation of each [1]. One or more additional energy sources, such as high voltage (HV) batteries for continuous electric energy demand and ultra capacitors for high peak power [2], provide the electric

power. Thus, in a hybrid electric vehicle, highly efficient and compact power electronic converters are required to provide the propulsion power and to facilitate the energy transfer between different dc voltage levels [3].

Now, the need for a bidirectional power converter should be properly examined. A battery can be used as a dc bus if the motor is rated for that voltage level. Thus, bidirectional power flow is not a problem because of the bidirectional power-handling capacity of a standard two-level three-phase inverter and also sinking and sourcing capacity of the battery. However, the traction motor should be rated for higher voltage to achieve higher efficiency for a given power rating. Therefore, the dc bus voltage should be maintained high enough to match the motor voltage rating. This problem can be solved by connecting a number of batteries in series. However, if too many batteries are connected in series, then the volumetric efficiency of the battery comes down. Therefore, there is a need for a bidirectional converter which interfaces the low-voltage battery with a high-voltage dc bus and maintains a bidirectional power flow.[2] shows the use of a bidirectional converter for a permanent-magnet ac motor- driven electric vehicle. [3] shows the use of a cascaded bidirectional buck–boost converter for the use in dc-motor-driven electric vehicle. Both schemes emphasize the importance of bidirectional dc–dc converter for electric vehicle application. The dc–dc converters can be divided into hard switching converters and soft-switching converters. Because of the low efficiency of hard-switching converters, recently, soft-switching techniques are getting popular. [4] proposes ZVS techniques for different non-isolated dc–dc converters. There is a limit on the voltage gain that can be achieved using a buck–boost or a boost converter. It is not desirable to operate the boost or the buck–boost converter at very high duty ratio because of very high capacitor current ripple. Thus, the solution is to go for isolated topologies for getting the high voltage gain in between the battery and the dc bus. In such topologies, any voltage gain can be achieved by setting the turns ratio of the transformers or the coupled inductors. Moreover, such topologies also provide the advantage of galvanic isolation between the battery bank and the dc bus. The recently proposed topologies mostly use soft-switching

techniques. [5] proposes a novel soft-switching topology for zeta–fly-back converter. [6] proposes a bidirectional dc–dc converter topology with dual half-bridge topology which has the advantage over dual full-bridge topology in terms of reduced device count. [7] proposes a bidirectional fly-back dc–dc converter with ZCS. The soft-switching topologies give higher efficiency at the cost of increased device count. Higher device count also reduces the reliability of the circuit. Now, if multiple batteries are to be connected in parallel to increase the total energy storage capacity, it is not possible by connecting the terminals of two batteries in parallel. This leads to the option of multiphase converter topology. Apart from giving the flexibility of paralleling multiple batteries, it also increases the fault-tolerant capacity, i.e., if one of the phases fails, then other phases can still operate, and the whole system will not come to a halt. [8] proposes a bidirectional dc–dc converter with many interleaved buck stages for automotive application. Apart from multiphase operation, the power converter should also be able to interface multiple energy sources to the battery. [9] proposes a scheme where multiple energy sources and the battery are connected to the dc bus, and the dc bus works as a junction point for all energy transfer.

II. CONCEPT OF FOUR PHASE BI-DIRECTIONAL FLYBACK CONVERTER

The basic block diagram of the prototype of the multi power port (MPP) which is built for hybrid electric vehicle application is shown in Figure 1. The heart of the circuit is the bidirectional fly-back dc–dc converter. A four-phase converter is constructed. The power schematic of the bidirectional dc–dc converter is shown in Figure 2. It has four identical bidirectional fly back dc–dc converters. Each converter has an individual battery, and all the converters are connected to the common dc bus. If we consider the first converter, then, during forward power flow S1 and D2 are active and during reverse power flow,

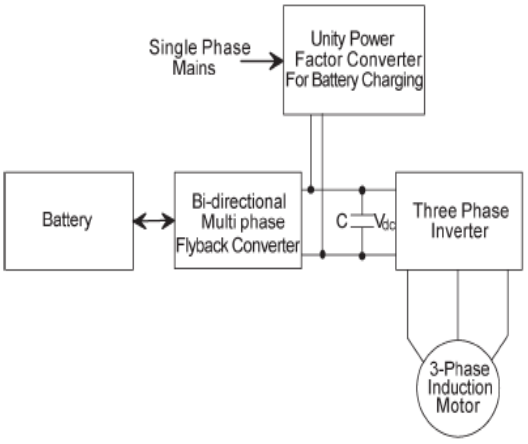


Figure 1. Block diagram of the proposed power schematic

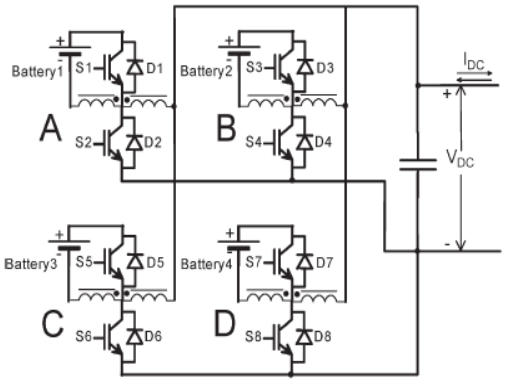


Figure 2: Four-phase bidirectional fly-back converter

S2 and D1 are active as well. During forward power flow, active switches S1, S3, S5, and S7 get switching pulses of 75% duty cycle with 90◦ phase difference between subsequent phases, as shown in Fig. 3(a). During reverse power flow, active switches S2, S4, S6, and S8 get switching pulses of 25% duty cycle which are 90◦ phase shifted to each other, as shown in Figure 3(b). Figure 3(c) and (d) shows the ideal switch voltage and current waveforms assuming continuous conduction mode (CCM) for forward and reverse power flows, respectively. CCM is not the only conduction mode for this bidirectional converter.

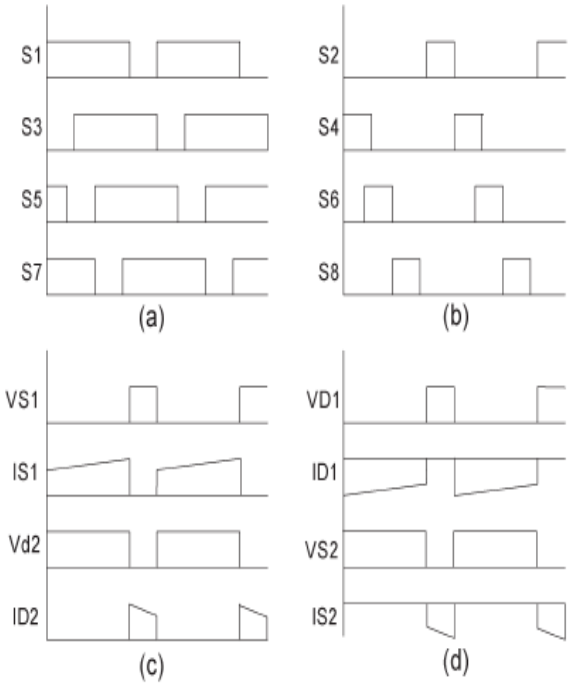


Figure 3: (a) Switching pulses during forward power flow. (b) Switching pulses during reverse power flow. (c) Ideal switch voltage and current waveforms during forward power flow for phase A assuming continuous conduction. (d) Ideal switch voltage and current waveforms during reverse power flow for phase A assuming continuous conduction.

This can also operate in critical conduction mode (CRM) or discontinuous conduction mode (DCM), depending on the load. During forward power flow, if the load is very less, then the converter can go into CRM or DCM, similar to any standard fly-back converter. However, for circuit design, only CCM is considered. As no snubber is used, circuit design involves the design of the inductor and the capacitor. The load connected at the output of the converter is a three phase inverter connected to the motor. Thus, the capacitor voltage ripple is dominated by the dc link current ripple of the inverter, and capacitor value is decided depending on that ripple. The fly-back inductor value is selected such that the inductor current ripple is 10% of the full-load current during CCM. DCM and CRM are not considered for circuit design because there is no stringent voltage regulation requirement for the MPP output. The regulation is handled by the downstream inverter.

III. CONTROL SCHEME

Simple hysteresis voltage control is used for dc-link voltage regulation for power management in the proposed MPP scheme. During power flow in the forward direction, i.e., from the battery to the dc bus, the duty cycles of switching voltages of S1, S3, S5, and S7 are fixed at 75%, while switches S2, S4, S6, and S8 are permanently off. During reverse power flow, S1, S3, S5, and S7 are permanently off, and S2, S4, S6, and S8 are switched at 25% duty cycle. Therefore, during forward power flow, the voltage is boosted by a factor of three, and during reverse power flow, the voltage is stepped down by a factor of three. It is to be noted that this voltage boost is only due to duty-cycle operation. The coupled-inductor turns ratio is fixed in such a way that during full-load operation in forward mode, the converter output voltage is the rated dc bus voltage V_{dc}. For an operating condition with lesser load, the series voltage drop in the converter will be less. Thus, the dc-link voltage will get increased from the rated value because of fixed duty cycle of operation. At a voltage $V_{dc} + v_1$, the pulses to switches S1, S3, S5, and S7 are stopped. If the load is still drawing current, then it will discharge the capacitor. When the voltage reaches V_{dc}, again, the switching pulses are given to S1, S3, S5, and S7. Therefore, during light-load conditions, the voltage is maintained between V_{dc} and $V_{dc} + v_1$. If there is no load, then the voltage will also be maintained in between V_{dc} and $V_{dc} + v_1$.

However, during regeneration, even if switches S1, S3, S5, and S7 are off, because of reverse power flow, the voltage will increase beyond $V_{dc} + v_1$. This is the time when energy should flow back to the battery. Thus, at a voltage $V_{dc} + v_1 + v_2$, switches S2, S4, S6, and S8 are pulsed, and because of the flyback action, current flows into the battery, and the battery gets charged. Here also, if the capacitor voltage falls below $V_{dc} + v_1$, the pulses to switches S2, S4, S6, and S8 are stopped. In this way, during regeneration, the voltage is maintained above $V_{dc} + v_1$. Here, the upper limit of the dc bus voltage is not fixed. It can be more than $V_{dc} + v_1 + v_2$ also if very high regenerative current flows. However, the rate at which the converter feeds current to the battery can be less because of fixed duty cycle of operation. Therefore, the capacitor voltage can shoot up to a very high value. The dynamic resistance of the inverter provides the necessary protection at this operating condition. The dynamic resistance of the inverter is activated when the capacitor voltage reaches $V_{dc} + v_1 + v_2 + v_3$. The dynamic resistor can be switched off when the capacitor voltage decreases below $V_{dc} + v_1 + v_2$. This same control scheme is exploited during the battery-charging operation. For battery charging, the front-end converter is designed to maintain a voltage more than $V_{dc} + v_1 + v_2$ but less than $V_{dc} + v_1 + v_2 + v_3$. Thus, automatically, the reverse-power-flow operation gets activated, and the battery gets charged.

IV. MATHEMATICAL MODEL OF INDUCTION MOTOR DRIVE

The induction machine d-q or dynamic equivalent circuit is shown in Fig. 3 and 4. One of the most popular induction motor models derived from this equivalent circuit is Krause's model detailed in [5]. According to his model, the modeling equations in flux linkage form are as follows:

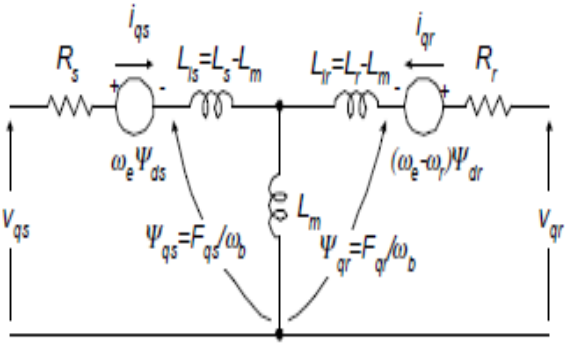


Figure 4: Dynamic q-axis model

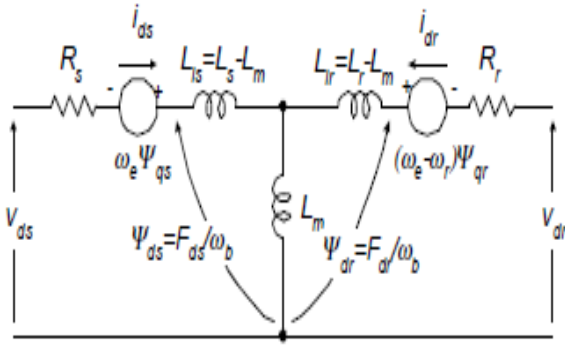


Figure 5: Dynamic d-axis model

$$\frac{dF_{qs}}{dt} = \omega_b \left[v_{qs} - \frac{\omega_e}{\omega_b} F_{ds} + \frac{R_s}{x_{ls}} \left(F_{mq} + F_{qs} \right) \right] \quad (1)$$

$$\frac{dF_{ds}}{dt} = \omega_b \left[v_{ds} + \frac{\omega_e}{\omega_b} F_{qs} + \frac{R_s}{x_{ls}} \left(F_{md} + F_{ds} \right) \right] \quad (2)$$

$$\frac{dF_{qr}}{dt} = \omega_b \left[v_{qr} - \frac{(\omega_e - \omega_r)}{\omega_b} F_{dr} + \frac{R_r}{x_{lr}} \left(F_{mq} - F_{qr} \right) \right] \quad (3)$$

$$\frac{dF_{dr}}{dt} = \omega_b \left[v_{dr} + \frac{(\omega_e - \omega_r)}{\omega_b} F_{qr} + \frac{R_r}{x_{lr}} \left(F_{md} - F_{dr} \right) \right] \quad (4)$$

$$F_{mq} = x^*_{ml} \left[\frac{F_{qs}}{x_{ls}} + \frac{F_{qr}}{x_{lr}} \right] \quad (5)$$

$$F_{md} = x^*_{ml} \left[\frac{F_{ds}}{x_{ls}} + \frac{F_{dr}}{x_{lr}} \right] \quad (6)$$

$$i_{qs} = \frac{1}{x_{ls}} \left(F_{qs} - F_{mq} \right) \quad (7)$$

where d : direct axis,
q : quadrature axis,
s : stator variable,
r : rotor variable,
F_{ij} is the flux linkage (i=q or d and j=s or r),
v_{qs}, v_{ds} : q and d–axis stator voltages,
v_{qr}, v_{dr} : q and d–axis rotor voltages,
F_{mq},F_{md} : q and d axis magnetizing flux linkages,
Rr : rotor resistance,
Rs : stator resistance,
X_{ls} : stator leakage reactance ($\omega_e L_{ls}$),
X_{lr} : rotor leakage reactance ($\omega_e L_{lr}$),

$$X_{ml}^{*} : 1 \Big/ \left(\frac{1}{x_m} + \frac{1}{x_{ls}} + \frac{1}{x_{lr}} \right),$$

i_{qs}, i_{ds} : q and d–axis stator currents,
i_{qr}, i_{dr} : q and d–axis rotor currents,
p : number of poles,
J : moment of inertia,
T_e : electrical output torque,
T_L(or T_l) : load torque,
ω_e : stator angular electrical frequency,
ω_b : motor angular electrical base frequency,
ω_r : rotor angular electrical speed.

$$i_{ds} = \frac{1}{x_{ls}} \left(F_{ds} - F_{md} \right) \quad (8)$$

$$i_{qr} = \frac{1}{x_{lr}} \left(F_{qr} - F_{mq} \right) \quad (9)$$

$$i_{dr} = \frac{1}{x_{lr}} \left(F_{dr} - F_{md} \right) \quad (10)$$

$$T_e = \frac{3}{2} \left(\frac{p}{2} \right) \frac{1}{\omega_b} \left(F_{ds} i_{qs} - F_{qs} i_{ds} \right) \quad (11)$$

$$T_e - T_L = J \left(\frac{2}{p} \right) \frac{d\omega_r}{dt} \quad (12)$$

For a squirrel cage induction machine, as in the case of this paper, v_{qr} and v_{dr} in (3) and (4) are set to zero. An induction machine model can be represented with five differential equations as shown. To solve these equations, they have to be rearranged in the state-space form, In this case, state-space form can be achieved by inserting (5) and (6) in (1–4) and collecting the similar terms together so that each state derivative is a function of only other state variables and model inputs. Then, the modeling equations (1-4) of a squirrel cage induction motor in state-space become

$$\frac{dF_{qs}}{dt} = \omega_b \left[v_{qs} - \frac{\omega_e}{\omega_b} F_{ds} + \frac{R_s}{x_{ls}} \left(\frac{x^*_{ml}}{x_{lr}} F_{qr} + \left(\frac{x^*_{ml}}{x_{ls}} - 1 \right) F_{qs} \right) \right] \quad (13)$$

$$\frac{dF_{ds}}{dt} = \omega_b \left[v_{ds} + \frac{\omega_e}{\omega_b} F_{qs} + \frac{R_s}{x_{ls}} \left(\frac{x^*_{ml}}{x_{lr}} F_{dr} + \left(\frac{x^*_{ml}}{x_{ls}} - 1 \right) F_{ds} \right) \right] \quad (14)$$

$$\frac{dF_{qr}}{dt} = \omega_b \left[-\frac{(\omega_e - \omega_r)}{\omega_b} F_{dr} + \frac{R_r}{x_{lr}} \left(\frac{x^*_{ml}}{x_{ls}} F_{qs} + \left(\frac{x^*_{ml}}{x_{lr}} - 1 \right) F_{qr} \right) \right] \quad (15)$$

$$\frac{dF_{dr}}{dt} = \omega_b \left[\frac{(\omega_e - \omega_r)}{\omega_b} F_{qr} + \frac{R_r}{x_{lr}} \left(\frac{x^*_{ml}}{x_{ls}} F_{ds} + \left(\frac{x^*_{ml}}{x_{lr}} - 1 \right) F_{dr} \right) \right] \quad (16)$$

$$\frac{d\omega_r}{dt} = \left(\frac{p}{2J} \right) \left(T_e - T_L \right) \quad (17)$$

V. MATLAB/SIMULINK MODELLING AND SIMULATION RESULTS

Here the simulation is carried out by two cases 1. Proposed Four-phase bidirectional fly-back converter 2. Proposed Four-phase bidirectional fly-back converter Applied to induction motor drive.

Case 1: Proposed Four-phase bidirectional fly-back

converter:

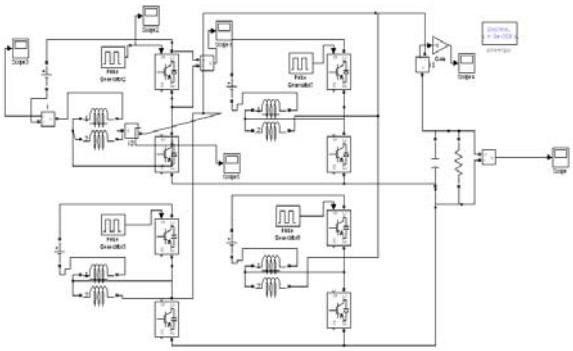


Figure 6: Matlab/Simulink model of Proposed Four-phase bidirectional fly-back converter without soft sort

Figure 6 shows the Matlab/Simulink model of Proposed Four-phase bidirectional fly-back converter without soft sort.

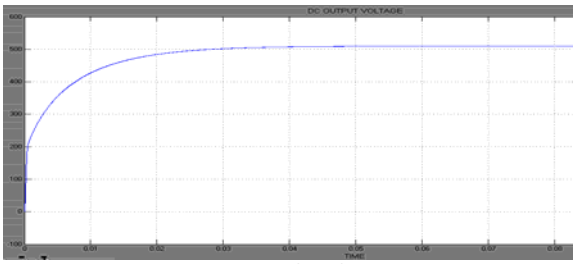


Figure 7: Output Voltage of the fly-back converter

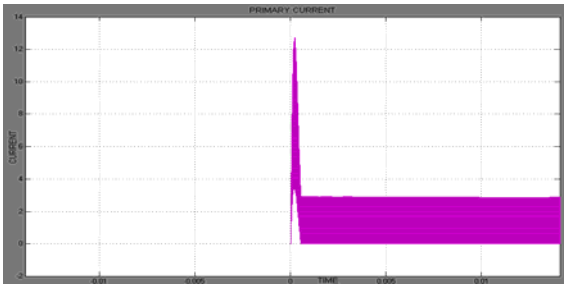


Figure 8: Primary current of the proposed fly- back converter without soft sort

Figure 7 and 8 shows the DC link voltage and Primary current of the proposed fly back converter without soft sort.

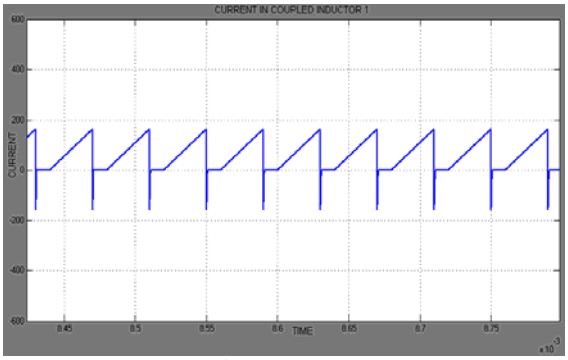


Figure 9: Current flowing in the coupled inductor

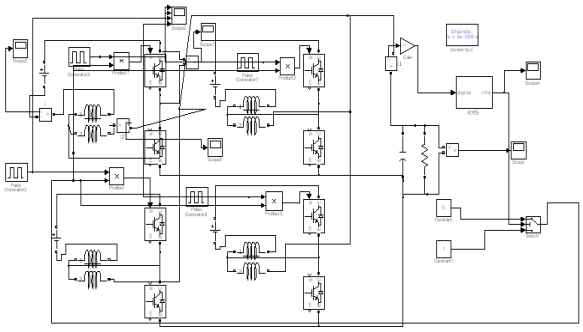


Figure 10: Matlab/Simulink model of Proposed Four-phase bidirectional fly-back converter with soft sort

Figure 10 shows the Matlab/Simulink model of Proposed Four-phase bidirectional fly-back converter with soft sort

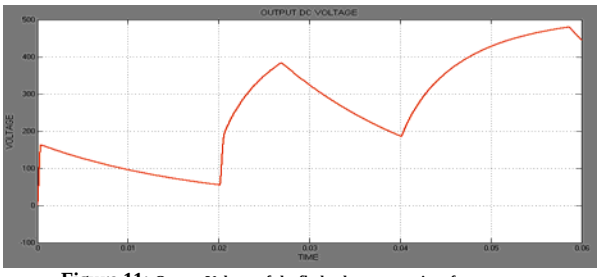


Figure 11: Output Voltage of the fly-back converter in soft sort

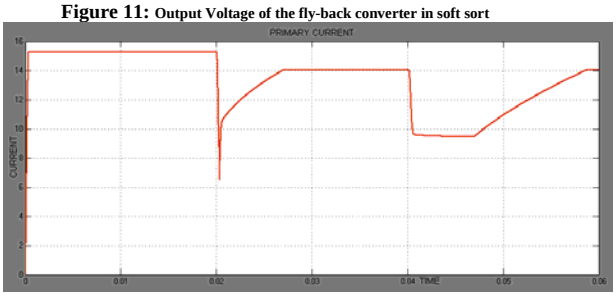


Figure 12: Primary Current of the fly back converter in soft sort

Figure 11 and 12 shows the DC Output voltage and primary current of the proposed fly back converter in soft sort method.

Case 2:. Proposed Four-phase bidirectional fly-back converter Applied to induction motor drive

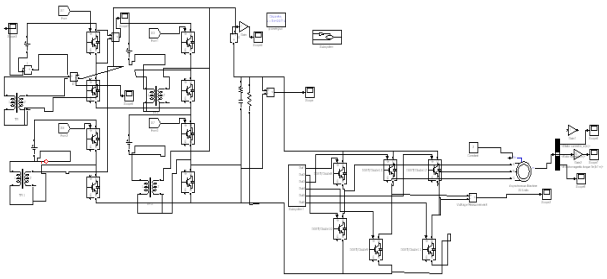


Figure 13: Matlab/Simulink Model of Proposed Four-phase bidirectional fly-back converter Applied to induction motor drive

Figure 13 shows the Matlab/Simulink model of Proposed Four-phase bidirectional fly-back converter Applied to induction motor drive interfacing by using the DC to AC converter. To check the performance of the induction motor drive.

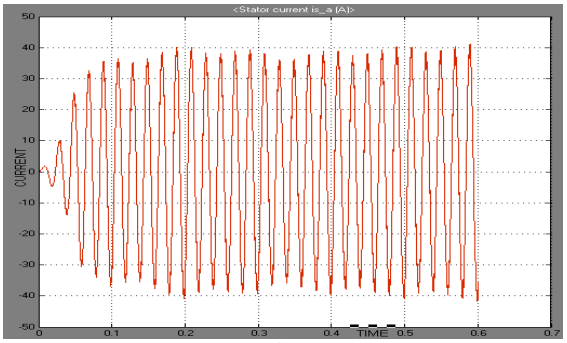


Figure 14: Stator Current of the Induction Motor Drive

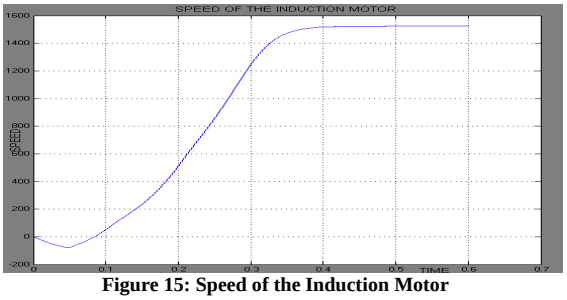


Figure 15: Speed of the Induction Motor

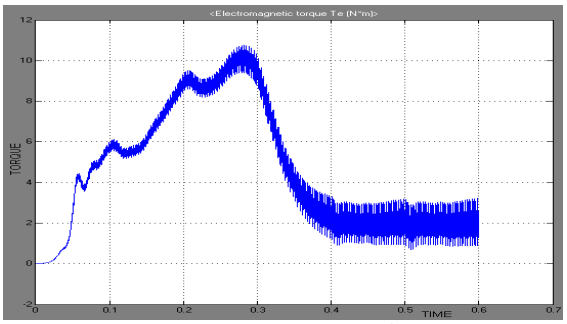


Figure 16: Electro-magnetic torque of the motor

Figure 14, 15, 16 Shows the Induction drive Performance Characteristics, Armature current, Speed , Electromagnetic Torque of the drive respectively.

V. CONCLUSION

This paper proposes a four-phase bidirectional fly-back dc–dc converter which serves the role of an MPP interface for electric and hybrid electric vehicle applications. The bidirectional nature of the converter allows battery charging during regeneration and also from mains. The multiple phases give the flexibility of paralleling multiple batteries. Simple hysteresis control is used for converter control. Because of the four converters operating with 90◦ phase shift with fixed 75% duty cycle of operation, the capacitor ripple current is also reduced. The novel transformer design technique drastically reduces the leakage inductance and eliminates the requirement of snubber. And same system is applied to Induction Motor Drive with the help of the interfacing inverter and to check the performance characteristics of system ,and drive.

REFERENCES

[1] A. Emadi, Y. J. Lee, and K. Rajashekara, “Power electronics and motordrives in electric, hybrid electric, and plug-in hybrid electric vehicles,” *IEEE Trans. Ind. Electron.*, vol. 55, no. 6, pp. 2237–2245, Jun. 2008.

[2] F. Caricchi, F. Crescimbini, G. Noia, and D. Pirolo, “Experimental study of a bidirectional DC–DC converter for the DC link voltage control and the regenerative braking in PM motor drives devoted to electrical vehicles,” in *Proc. IEEE APEC*, Orlando, FL, Feb. 1994, vol. 1, pp. 381–386.

[3] F. Caricchi, F. Crescimbini, F. G. Capponi, and L. Solero, “Study of bi-directional buck–boost converter topologies for application in electrical vehicle motor drives,” in *Proc. IEEE APEC*, Feb. 1998, vol. 1, pp. 287–293.

[4] C.-M. Wang, “Novel zero-voltage-transition PWM DC–DC converters,” *IEEE Trans. Ind. Electron.*, vol. 53, no. 1, pp. 254–262, Feb. 2006.

[5] B.-R. Lin and F.-Y. Hsieh, “Soft-switching zeta–flyback converter with a buck–boost type of active clamp,” *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2813–2822, Oct. 2007.

[6] F. Z. Peng, H. Li, G.-J. Su, and J. S. Lawler, “A new ZVS bidirectional DC–DC converter for fuel cell and battery application,” *IEEE Trans. Power Electron*, vol. 19, no. 1, pp. 54–65, Jan. 2004.

[7] H. S.-H. Chung, W.-L. Cheung, and K. S. Tang, “A ZCS bidirectional flyback DC/DC converter,” *IEEE Trans. Power Electron*, vol. 19, no. 6, pp. 1426–2434, Nov. 2004.

[8] O. Garcia, P. Zumel, A. de Castro, and J. A. Cobos, “Automotive DC–DC bidirectional converter made with many interleaved buck stages,” *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 578–586, May 2006.

[9] L. Solero, A. Lidozzi, and J. A. Pomilio, “Design of multiple-input power converter for hybrid vehicles,” in *Proc. IEEE APEC*, vol. 2, pp. 1145–1151.

[10] M. Michon, J. L. Duarte, and M. Hendrix, “A three port bi-directional converter for hybrid fuel cell systems,” in *Proc. IEEE PESC*, Aachen, Germany, Jun. 2004, pp. 4736–4742.

[11] H. Tao, A. Kotsopoulos, J. L. Duarte, and M. A. M. Hendrix, “Family of multiport bidirectional DC–DC converters,” *Proc. Inst. Elect. Eng.—Electr. Power Appl.*, vol. 153, no. 3, pp. 451–458, May 2006.

[12] R.-J. Wai, L.-W. Liu, and R.-Y. Duan, “High-efficiency voltage-clamped DC–DC converter with reduced reverse-recovery current and switch voltage stress,” *IEEE Trans. Ind. Electron.*, vol. 53, no. 1, pp. 272–280, Feb. 2006.

[13] R.-J. Wai, C.-Y. Lin, R.-Y. Duan, and Y.-R. Chang, “High-efficiency DC–DC converter with high voltage gain and reduced switch stress,” *IEEE Trans. Ind. Electron.*, vol. 54, no. 1, pp. 354–364, Feb. 2007.

[14] T. Bhattacharya, V. S. Giri, K. Mathew, and L. Umanand, “Multi power port converter for hybrid electric vehicles using multi phase bidirectional fly-back topology,” in *Proc. IEEE ICIT*, Dec. 2006, pp. 1201–1205.

◈◈◈

MODELING ASPECTS OF CARBON NANOTUBE FIELD EFFECT TRANSISTORS

[1]SRIDEVI V. & [2]JAYANTHY T.

[1]Research Schola,r, Sathyabama University, Chennai, India.
[2]Panimalar Institute of Technology, Chennai, India.

Abstract— Carbon Nanotube Field Effect Transistor is a promising device to supersede the MOSFET at the end of the technology roadmap of complementary MOS. Since the first CNTFET was reported in 1998, measureless progress has been made during the past years in all the areas of CNTFET science and technology including materials, devices and circuits. The ultimate purpose of this paper is to investigate the modeling of CNTFETs (both coaxially gated and MOSFET like CNTFET) and to explore their variation in performance with variations in the device structure such as CNTs diameter, gate dielectric thickness, contact resistances etc. With this information, a better CNTFET can be designed and effectively used for carbon nanotube technology. In this paper, two different CNTFET models (coaxially gated and MOSFET-like) have been developed and implemented in MATLAB (coaxially gated CNTFET) and HSPICE (MOSFET-like CNTFET). By analysing the simulation results of both CNTFETs, it has been concluded that MOSFET like CNTFET will deliver more current than SB CNTFET and is best suited for designing analog and digital circuits.

Keywords *- Coaxially gated; MOSFET like CNTFET; MATLAB; HSPICE;Simulation.*

I. INTRODUCTION

For many years MOSFET has been used as a basic element of circuit designing[1]. As the miniaturization of silicon based circuits reaches its physical limitations, molecular devices are becoming hopeful alternatives to the existing silicon technology [2][3]. Carbon Nano Tube (CNT) technology is at the front of these technologies due to the unique mechanical and electronic properties. Semi-conducting carbon nanotube can be used as the channel in Carbon Nanotube Field Effect Transistor (CNTFET).

CNTFETs are novel devices that are expected to sustain the transistor scalability while increasing its performance. One of the major differences between CNTFETs and MOSFETs is that the channel of the former devices is formed by CNTs instead of silicon, which enables a higher drive current density, due to the larger current carrier mobility in CNTs compared to bulk silicon[4]-[6].The main drawbacks of the MOSFET is that the sensitivity of a MOSFET's gate to static and high-voltage spikes makes it vulnerable to damage resulting from parasitic oscillation. This undesired self-oscillation could result in excessive gate-to-source voltage that permanently damages the MOSFET's gate insulation. Another MOSFET limitation is gate capacitance. This parameter limits the frequency at which a MOSFET can operate effectively. CNTFET overcomes these limitations to produce better performance than MOSFET.

In this paper, section II deals with the structure, modeling aspects of coaxially gated CNTFET and MOSFET like CNTFET. By analyzing the simulation results of both CNTFETs in Section III it has been concluded in Section IV that MOSFET like CNTFET will deliver more current than SB CNTFET and is best suited for designing analog and digital circuits

II. MODELING ASPECTS OF CNTFET

A Carbon Nanotube Field Effect Transistor (CNTFET) is formed by connecting two metal electrodes on the either side of the CNT that forms source and drain contacts with gate electrode separated from the nanotube by a thin oxide film. In this work two types of CNTFETs i.e. coaxially gated type and MOSFET like type have been modeled and analysed.

A. Coaxially gated CNTFET

In a coaxially gated CNTFET shown in Figure 1, the gate of the CNTFET encapsulates the entire channel. A carbon nanotube of radius R_{CNT} forming the channel of CNTFET is surrounded by cylindrical gate of radius R_g. A layer of cylindrical dielectric (Silica, Zirconia or Alumina) separates the tube and the gate electrode. The behaviour of CNTFET is decided by the tube dimensions (R_{CNT} and L_{CNT}), the gate dielectric thickness, thickness of metal contacts and work functions of the source, drain and gate metals [7-14].

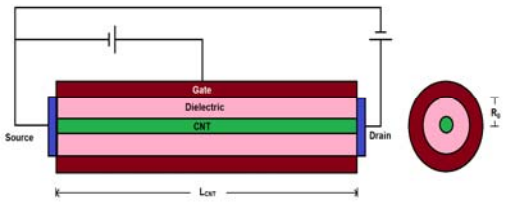


Figure 1. Structure of Coaxially gated CNTFET

Figure 2 shows the circuit arrangement for one dimensional n-type model.

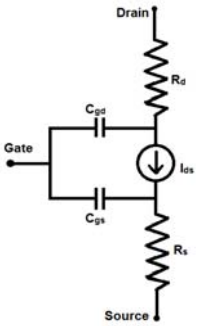


Figure 2. Circuit model of CNTFET

The current expression for the model can be implemented as

$$\Psi_s = V_{gs} - U \quad (1)$$

$$\xi_S = \frac{(\Psi_s - \Delta)}{k_B T} \quad (2)$$

$$\xi_D = \frac{(\Psi_s - \Delta - V_{ds})}{k_B T} \quad (3)$$

$$I_D = \frac{4qk_B T}{h}\left[\ln(1+\exp(-\xi_S)) - \ln(1+\exp(-\xi_D))\right] \quad (4)$$

$$I_t = \frac{8e^2}{h}\cdot\exp(-\frac{E_g}{2k_B T})\cdot V_{ds} \quad (5)$$

$$I = \begin{cases} I_D + I_t & for \quad V_{gs} > V_{th} \\ 0 & for \quad V_{gs} < V_{th} \end{cases} \quad (6)$$

where $\xi_i = \left(\frac{\Psi_s - \Delta - \mu_i}{k_B T}\right)$ for i = S, D and Δ is the half band gap energy and μ_i is '0' and $-qV_{ds}$ respectively for source and drain. Ψ_s is given by V_{gs}-U, where U is the local potential.

In the above circuit model, all the parasitic resistances and capacitances have been neglected. The interconnect capacitors and the gate-source and gate-drain overlap capacitors are the significant parasitic capacitors in the design. Likewise, the electrode resistances (R_s and R_d) play an important role in the delay characteristics of a CNTFET based circuit.

B. MOSFET like CNTFET

Figure 3 shows a typical structure of MOSFET like CNTFET with single carbon nanotube. Multiple CNTs can be placed under the same gate for improving the drive current. The semiconducting CNT acts as a undoped channel region whereas the source and drain regions are heavily doped.

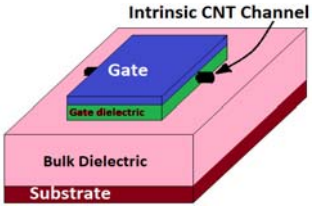


Figure 3. Structure of MOSFET like CNTFET

The equivalent circuit model of MOSFET like CNTFET is shown in Figure 4. It consists of 3 current sources and 5 transcapacitance network to account for both dc and ac behavior of CNTFET.

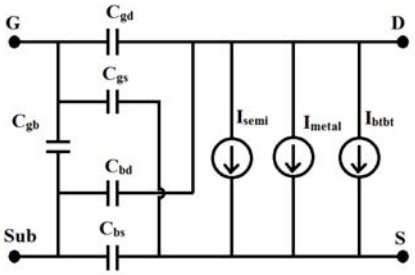


Figure 4. Equivalent circuit of CNTFET

In this paper, the SWCNT is treated as quasi 1-D quantum wire [15] [16]. In the model shown in Figure 4 , We have considered three current sources, (i)Thermionic current contributed by the semiconducting sub-bands (I_{semi}), (ii) Current contributed by metallic subbands (I_{metal}) and (iii) Leakage current contributed by the band to band tunnelling mechanism through the semiconducting sub-bands.

The thermionic current contributed by the semi conducting sub-bands Isemi is given by,

$$I_{semi}(V_{ch,DS}, V_{ch,GS}) = \frac{4e^2}{h}\sum_{\substack{m \\ m=1}}^{M} k_m T_m \left[V_{ch,DS} + \frac{kT}{e}\ln\left(\frac{1+e^{(E_{m,0}-\Delta\Phi_B)/kT}}{1+e^{(E_{m,0}-\Delta\Phi_B+eV_{ch,DS})/kT}}\right)\right]$$

(7) $V_{ch,DS}$ and $V_{ch,GS}$ denotes the Fermi potential differences near source side within the channel, e is the unit electronic charge, $\Delta\Phi_B$ is the channel surface potential change with gate/drain bias, T_{metal} is the transmission probably, k is the Boltzmann constant and T is the temperature in Kelvin and $E_{m,0}$ is the half band gap of the m^{th} sub-band.

For metallic sub-bands of metallic nanotubes, the current Imetal includes both the electron current and the hole current,

$$I_{metal} = 2(1-m0)T_{metal}\sum_{\substack{l \\ l=1}}^{L} k_l \left[J_{ele\_0,l} + J_{hole\_0,l}\right] \quad (8)$$

$$J_{ele\_0,l} = \frac{2e}{h}\frac{\sqrt{3}a\pi V_\pi}{L_g}\left(f_{FD}(E_{0,l}-\Delta\Phi_B) - f_{FD}(E_{0,l}+eV_{ch,DS}-\Delta\Phi_B)\right) \quad (9)$$

$$J_{hole\_0,l} = \frac{2e}{h}\frac{\sqrt{3}a\pi V_{\pi}}{L_g}\left(f_{FD}(-E_{0,l}-\Delta\Phi_B)-f_{FD}(-E_{0,l}+eV_{ch,DS}-\Delta\Phi_B)\right)$$

(10)

$f_{FD}(E)$ is the Fermi-Dirac distribution function,

$$f_{FD}(E) = \frac{1}{1+e^{E/kT}}$$

(11)

and the transmission probability T_{metal} is given by,

$$T_{metal} = \frac{\lambda_{ap}\lambda_{op}}{\lambda_{ap}\lambda_{op}+(\lambda_{ap}+\lambda_{op}).L_g}$$

(12)

L_g, the channel length , λ_{op} (~ 15 nm[17]), the optical phonon scattering mean free path (MFP) and λ_{ap} (~ 500 nm[18]), the acoustic phonon scattering MFP.

In the sub-threshold region, especially with negative gate bias (nFET), the band-to-band tunneling current from drain to source becomes significant. We include a voltage controlled current source I_{btbt} in the device model in order to evaluate the device sub-threshold behavior and the static power consumption.

$$I_{btbt} = \frac{4e}{h}kT\sum_{m=1}^{M}k_m T_{btbt}\ln\left[\left(\frac{1+e^{(eV_{ch,DS}-E_{m,0}-E_f)/kT}}{1+e^{(E_{m,0}-E_f)/kT}}\right)\cdot\frac{\max(eV_{ch,DS}-2E_{m,0},0)}{eV_{ch,DS}-2E_{m,0}}\right]$$

(13)

III. RESULTS AND DISCUSSION

A. *Coaxially Gated CNTFET*

The parameters used for the model are given below.

- Nanotube Radius: R_t = 0.6nm
- Length of the tube: L_t = 100nm
- Gate Dielectric Thickness: R_g = 6.0nm
- SWNT Work function = Source/drain/gate metal work function = 4.5eV
- Gate Insulator = Zirconium
- Operating temperature = 300K

a) Density of States

The simulation of the DOS for the lowest sub-band of a typical SWCNT shows a symmetric density of states around the Fermi level with the maxima at just above the conduction band and just below the valence band respectively as shown in Figure 5.

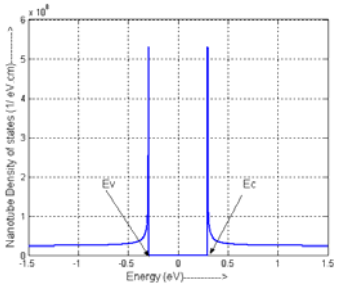


Figure 5. Nanotube Density of States

b) Charge Density

The Figure 6 shown below gives us an idea about how the charges developed inside the Nanotube get effected by varying gate voltage. Charge density is given by the product of the number of states present (i.e., Density of States) and the probability of electron present in those states (i.e., Fermi-Dirac probability). As expected we can see that the charge density increases as we increase the gate potential as the Fermi level moves closer to the valence band.

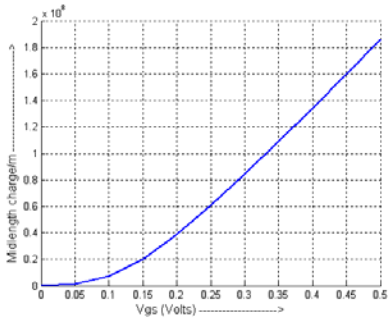


Figure 6. Charge Density with varying Vgs

c) Gate Insulator Thickness

Figure 7 shows that as the ratio of the gate dielectric radius to the SWCNT radius increases, the charge induced on the nanotube is reduced, since capacitance is inversely proportional to the distance between the plates. It follows that the charge induced on the channel must reduce for increasing thickness of the gate dielectric. This can simply be viewed as a reduction in the ability of the gate to control the channel as it is moved further away from it. Thus, as the gate dielectric is made thinner, the gate has better control over the channel.

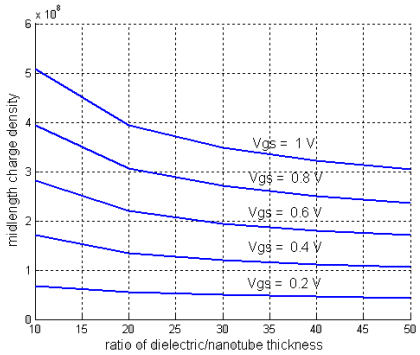


Figure 7. Charge induced on the gate as a function of dielectric thickness and Vgs

d) Bipolar Current Characteristics

Figure 8 shows the bipolar I-V characteristics respectively of SB-CNTFET which includes contribution due to the thermionic current.

As the drain voltage is increased beyond the half bandgap value of SWCNT, the barrier for electrons at the drain is entirely suppressed and now a tunneling barrier begins to form for the holes. This leads to a net bipolar current that has contribution

from the electrons injected into the channel from the source as well as holes injected into the channel from the drain. As V_{ds} keeps increasing, the hole current begins to increase until the point where V_{ds} is equal to the valence band edge of the SWCNT. At this point, the contribution due to the hole current equals that of the electron current and for a higher V_{ds}, the hole current exceeds the electron current in magnitude.

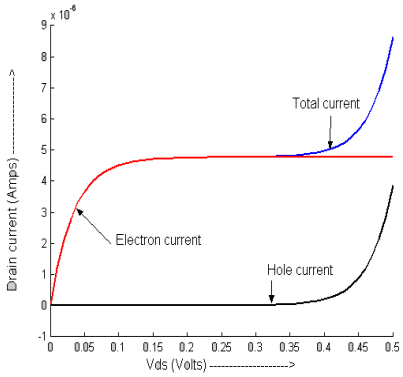


Figure 8. Bipolar IV Characteristics of SB CNTFET

Ambipolar conduction gives rise to larger leakage current that increases exponentially with the power supply voltage, particularly when the tube diameter is large. SB CNTFET suffer from the necessity to place the gate electrode close to the source (increases parasitic capacitance) and induced gap states which increases the source to drain tunnelling and reduces the minimum channel length. By using heavily doped CNT section as source and drain, ambipolar conduction will be suppressed with reduction in leakage current and the scaling limit imposed by source/drain tunnelling will be extended. MOSFET like CNTFET in turn suppress the ambipolar conduction that occurs in SB CNTFET and also extends the channel length scaling limit. The parasitic capacitance between the source and gate electrode will also be reduced leading to faster operation and the leakage current is controlled by the full band gap of CNTs and band to band tunneling

B. MOSFET like CNTFET

We build a HSPICE model for MOSFET like CNTFET targeting at some important device parameters such as physical channel length(L_{ch}), coupling capacitance between channel region and substrate(C_{sub}), fermi level of doped S/D tube(E_f), gate dielectric thickness(H_{ox}), number of tubes etc to determine how best to optimize the device. The resultant drain currents by varying the targeted parameters are shown in Figure (9-13).

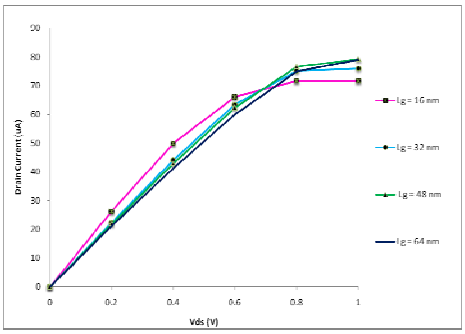


Figure 9. Drain Current in uA for various values of channel length and V_{ds}

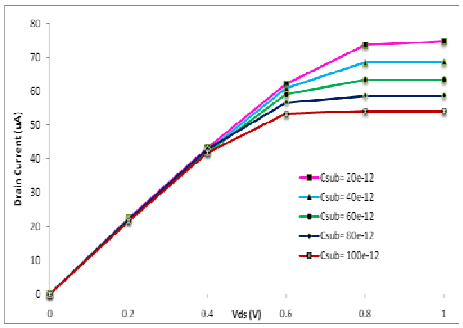


Figure 10. Drain Current in uA for various values of C_{sub} and V_{ds}

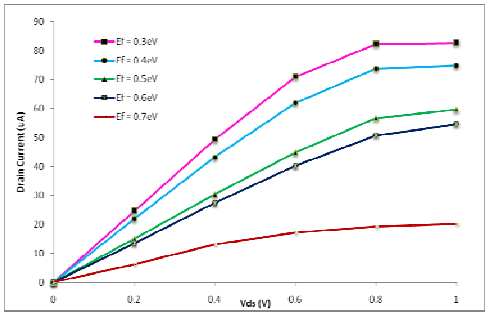


Figure 11. Drain Current in uA for various values of E_f and V_{ds}

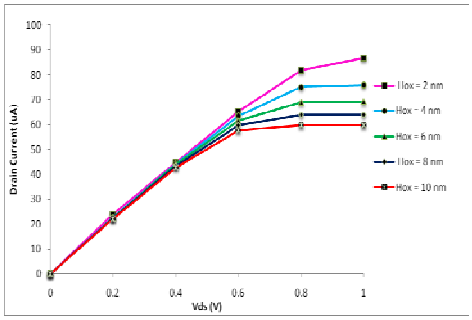


Figure 12. Drain Current in uA for various values of H_{ox} and V_{ds}

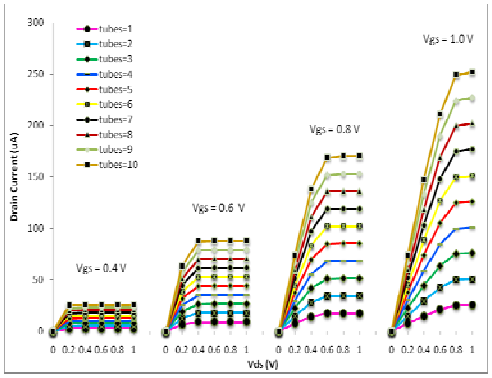


Figure 13. Drain Current in µA for various values of V_{gs}, V_{ds} and no of Tubes

By choosing the best values for the parameters from the simulated results, a complete model with high fabrication feasibility and superior device performance was developed for CNTFET. The parameters of the developed CNTFET model and their values with brief description are shown in Table 1.

TABLE I. CNTFET MODEL PARAMETERS

Parameter	Description	Value
Lch	Physical channel length	32nm
Lgeff	The mean free path in the intrinsic CNT channel	100nm
Lss	The length of doped CNT source-side extension region	32nm
Ldd	The length of doped CNT drain-side extension region	32nm
Kgate	The dielectric constant of high-k top gate dielectric material	16
n1,n2	The chirality of the tube	19,0
Tox	The thickness of high-k top gate dielectric material	4nm
Csub	The coupling capacitance between the channel region and the substrate	20pF/m
Kox	Gate Dielectric constant (HfO2)	16
VDD	Supply Voltage	1V
Ef	The Fermi level of the doped S/D tube	0.6eV
Hox	The gate dielectric thickness between the SWCNT center and gate	4nm

Figure 14 and Figure 15 shows the output characteristics of the developed CNTFET without and with non-idealities for different applied gate voltage. For this we have considered a CNTFET with a (19, 0) zig-zag CNT as the channel and channel length of 32nm. The various non-idealities taken into account are resistance and capacitance of doped S/D CNT region, SB resistance of S/D contacts and capacitance and screening due to multiple CNTs. The range of drain voltage is from 0V to 0.9V and the plots are for gate voltages 0.2V till 0.9V with an increment of 0.1V. For example, If we compare the two curves for Vgs=0.9V, in the curve without non-idealities saturation region starts almost from 0.3V with an on-current of ~34µA whereas in the curve with non-idealities the saturation region starts from 0.65V with a reduced on-current of ~20µA.

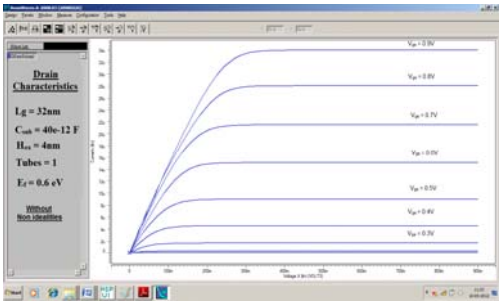


Figure 14. Drain characteristics of CNTFET – without non idealities

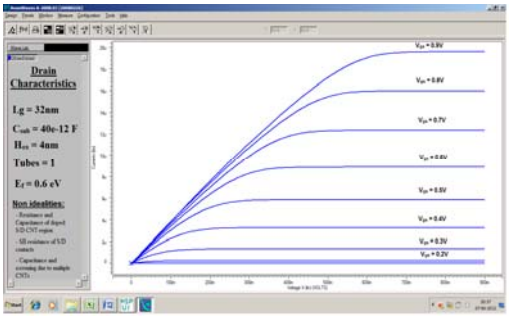


Figure 15. Drain characteristics of CNTFET – with non idealities

IV. CONCLUSION

This paper presents circuit compatible models for single walled Carbon Nanotube Field Effect Transistor. The coaxially gated CNTFET model was implemented and simulated in MATLAB which effectively explains the working of SB CNTFET and also explains the bipolar nature of current flow in the transistor. The simulation results shows that, good dc current can be achieved by SB CNTFET with its self aligned structure, but its ac performance is going to be poor due to the proximity of the gate electrode to the source drain metal. Also, the ambipolar behavior of SB CNTFET makes it undesirable for complementary logic design. On the other hand, MOSFET like CNTFET exhibits unipolar behavior by suppressing either electron (pCNTFET) or hole (nCNTFET) transport with heavily doped source and drain contacts. By considering the fabrication feasibility and superior device performance of MOSFET like

CNTFET as compared to SB-CNTFET, we then focussed on MOSFET-like CNTFETs. The simulations have been carried out with variations in the parameters such as physical channel length (L_{ch}), coupling capacitance between channel region and substrate (C_{sub}), fermi level of doped S/D tube (E_f), gate dielectric thickness (H_{ox}) etc.

REFERENCES

[1] Mojtaba Jamalizadeh, Fazel Sharifi, Mohammad Hossein Moaiyeri, Keivan Navi and Omid Hashemipour,"Five new MVL current mode differential absolute value circuits based on carbon nano-tube field effect transistors (CNTFETs)" Nano-Micro letters, Vol. 2, No. 4,2010, 227-234.

[2] Joerg Appenzeller, Joachim Knoch, Richard Martel, Vincent Derycke, Shalom J.Wind, and Phaedon Avouris, "Carbon Nanotube Electronics", IEEE Trans. on Nano Technology, 2002, pp. 184 –189.

[3] T. Dang, L. Anghel, R. Leveugle, "CNTFET Basics and Simulation", IEEE Trans. Elec.dev., 2006.

[4] H.-S. P. Wong, "Beyond the Conventional Transistor," IBM J. Research & Development, March/May, pp. 133-168, 2002.

[5] T. Skotnicki, J. A. Hutchby, T.-J. King, H.-S. P. Wong, F. Beouff, "The Road to the End of CMOS Scaling," IEEE Circuits and Devices Magazine, pp. 16 – 26, 2005.

[6] A. Javey, J. Guo, D. B. Farmer, Q. Wang, E. Yenilmez, R. G. Gordon, M. Lundstrom, H. Dai, "Self-Aligned Ballistic Molecular Transistors and Electrically Parallel Nanotube Arrays," Nano Letters, vol. 4, pp. 1319-1322, 2004.

[7] Fabien Pr´egaldiny et.al.,"Compact Modeling and Applications of CNTFETs for Analog and Digital Circuit Design", IEEE Trans. Elec.dev., pp. 1030–1033, 2006.

[8] Fabien Pr´egaldiny et.al.,"Design Oriented Compact Models for CNTFETs", IEEE Trans. Elec.dev., 2006.

[9] Paul L.McEuen, Michael Fuhrer, Hongkun Park, "Single walled carbon nano tube Electronics", IEEE Trans. on Nano Technology, 2002.

[10] S. Heinze, J. Tersoff, R. Martel, V. Derycke, J.Appenzeller, and P.Avouris, "Carbon nanotubes as Schottky barrier transistors," Phys. Rev.Lett., vol. 89, no. 10, pp. 106 801-1–106 801-4, 2002.

[11] J. Appenzeller, J. Knoch, V. Derycke, R. Martel, S. Wind, and P.Avouris, "Field-modulated carrier transport in carbon nanotube transistors,"Phys. Rev. Lett., vol. 89, no. 12, pp. 126 801-1–126 801-4, 2002.

[12] Jason Clifford, D. L. John, , and David L. Pulfrey, "Bipolar Conduction and Drain-Induced Barrier Thinning in Carbon Nanotube FETs", IEEE Trans. on Nano Technology, pp. 181 –185, 2003.

[13] D. L. John, L. C. Castro, J. P. Clifford, and D. L. Pulfrey, "Electrostatics of coaxial Schottky-barrier nanotube field-effect transistors," IEEE Trans. Nanotechnol., vol. 2, pp. 175–180, 2003.

[14] Arash Hazeghi, Tejas Krishnamohan, and H.-S. Philip Wong,"Schottky-Barrier Carbon Nanotube Field-Effect Transistor Modeling", IEEE Trans. Electron Devices, vol. 54, no. 12, pp. 439–445,Mar. 2007.

[15] Jie Deng, Albert Lin, Gordon C.Wan and H.S. Philip Wong," Carbon Nanotube Transistor compact model for circuit design and performance optimization", Applied Physics Letters, 290(5496), 1552-1555, 2000.

[16] Jie Deng and H.S. Philip Wong," Modeling and analysis of planar-gate electrostatic capacitance of 1-D FET with multiple cylindrical conducting channels", IEEE Transactions on Electron Devices, 54, 2377-2385, 2007.

[17] A. Javey et al., (2004b) 'High-Field Quasiballistic Transport in Short Carbon Nanotubes', Physical Review Letters, vo. 92, pp. 106804.

[18] J. Guo and M. Lundstrom, (2005) 'Role of Phonon Scattering In Carbon Nanotube Field-Effect Transistors', Applied Physics Letters, vol. 86, pp. 193103.

◈◈◈

RADIO FREQUENCY IDENTIFICATION UHF TAG USING RCEAT

BOYINA SWATHY & K MURTHY RAJU

Sri Vishnu womens Engineering College, JNTU, Kakinada

Abstract: - Radio Frequency Identification (RFID) UHF Tag based on RCEAT technique is proposed in this paper. RCEAT means Reliable and Cost Effective Anti-collision technique. The proposed system is designed with the help of Verilog HDL. The System is simulated using Modelsim SE 6.3f and it synthesized using XST. The RCEAT system is classified into two subsystems. One is Pre and another one is Post . By using Pre we have to detect the errors from incoming messages. And using Post we identify the tag.

Key words*: Verilog HDL,CRC remover, Fast-search look up table,Xlinx ise.*

1. INTRODUCTION

A significant advantage of RFID devices over the others identification devices is that the RFID device does not need to be positioned precisely relative to the scanner. As credit cards and ATM cards must be swiped through a special reader. In contrast, RFID devices will work within a few feet (up to 20 feet for high-frequency devices) of the scanner. But the problem associated with this technique is the collision of tags. So inorder to avoid coliision of tags a technique has been proposed which is both reliable and also cost effective. And so call this technique as Reliable and Cost Effective Anti-Collision Technique(RECEAT). This proposed technique does not require the tag to remember the instructions from the reader during the identification process. Thus the tag is treated as an address carrying device only and memory-less tag can be designed which requires very low power.

Some common problems with RFID are reader collision and tag collision. Reader collision occurs when the signals from two or more readers overlap. The tag is unable to respond to simultaneous queries. Systems must be carefully set up to avoid this problem. Tag collision occurs when many tags are present in a small area; but since the read time is very fast, it is easier for vendors to develop systems that ensure that tags respond one at a time.

The tag collision can be eliminated using different techniques.They are mainly of two types: a)Tree Based Algorithms and ALOHA based algorithms. where Tree based algoritms consists of Binary tree algorithms and Query tree. Whereas the ALOHA based algorithms are classified into ALOHA,Slotted ALOHA and Frame Slotted ALOHA. Some hardwares also desigened for this purpose. Here in this paper Tree algorithms has been considered with Fast Search Algorithm.

2. ARCHITECTURE :

The architecture consists of two parts:Pre RECEAT and Post RECEAT. The first part,the PRE RECEAT ensures that the incoming messages are errorless using a CRC-remover. In the CRC-remover the incoming messages are divided into two;the received ID and CRC. These two are sent to CRC checker for verification process where the received CRC is being checked with the recalcalucated CRC of the received message. If both are equal means no error and this is indicated by status bit which is set to zero. Otherwise the status bit is set to two. And then the status bit is updated and sent to status checker. If no errors are present then it is sent to the next part;the Post RECEAT part.

In PostRCEAT, the active tags are divided into a group of four for every Read cycle in order to reduce the number of iterations in the identification process. The PostRCEAT reads all the ID bits at once regardless of its length. This is performed by using the word-by word multiplexing. During the identification process, the Fast-search module identifies the four tag's IDs simultaneously in one Read cycle. The module firstly identifies the smallest ID bits until the largest one follows the Binary Tree with a maximum number of four leaves.

To avoid the four incoming packets from colliding with each other, these packets (IDs) are identified using the Binary Tree based technique with maximum four leaves. The reader selects these IDs using the proposed Fast-search Lookup table, and then the selected ID will be identified. The four IDs will be identified from the smallest value to the largest one in one Read cycle. Then the tag that has successfully identified will be acknowledged by sending the Kill-tag.

Once the tags are identified the most significant bit is represented by 1,which specifies that the tags are

identified. So we use Cyclic Redundant Check for getting errorless incoming messages and then those are checked with the recalculated one and then goes to the Post part where using fast search algorithm four tags are considered at once then arranged into ascending order ,then comes out one by one using a parallel to serial converter. Which will be the final output which is both reliable and cost effective.

The whole process can be represented simply by using a block diagram as:

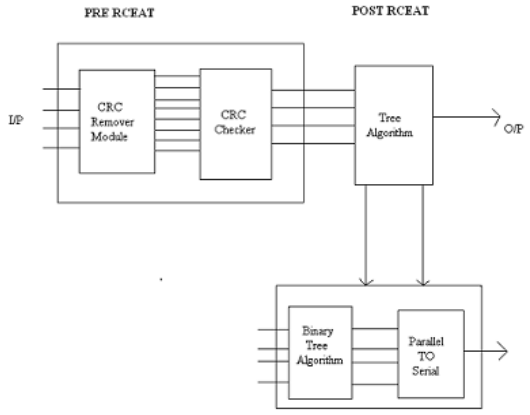
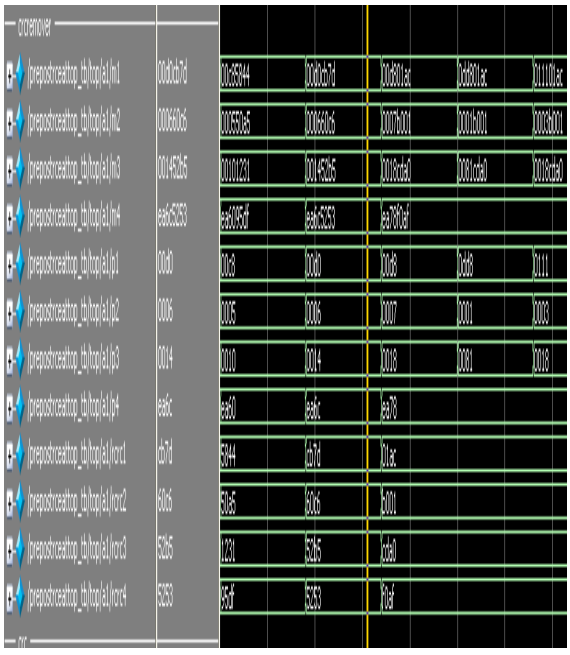


Fig:simple block diagram representation

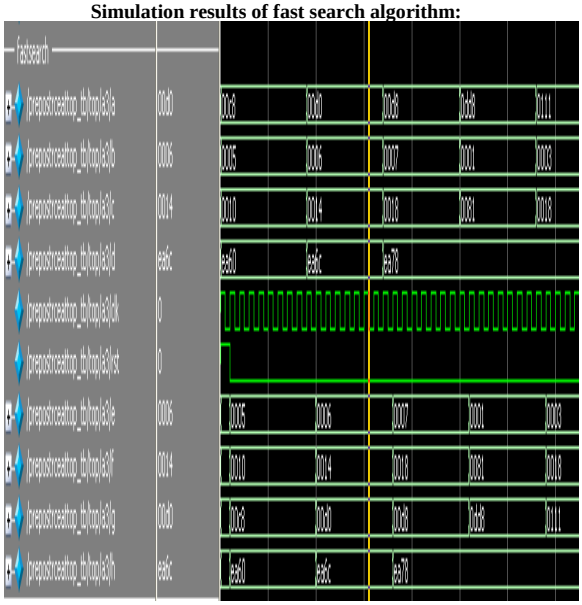
3. SIMULATION RESULTS:

The proposed technique has been simulated and verified using Modelsim and synthesized usisg Xlinx ISE and obtained the results. The obtained results are also shown:

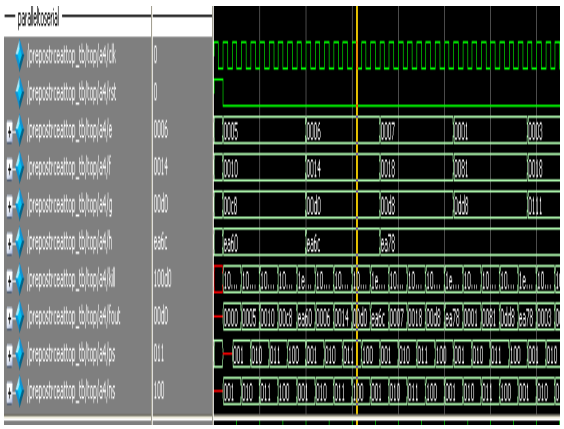
Simulation Results of crcremover :



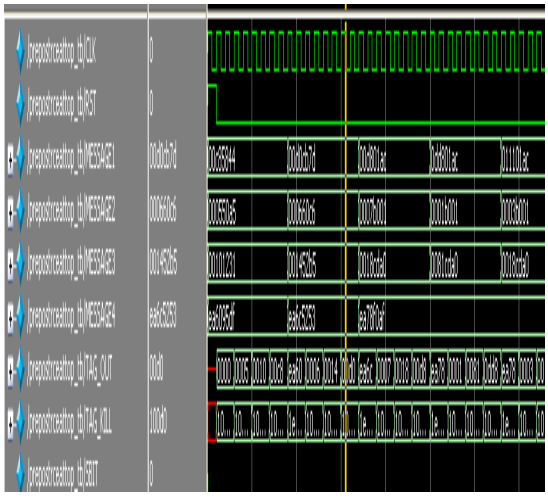
Simulation results of fast search algorithm:



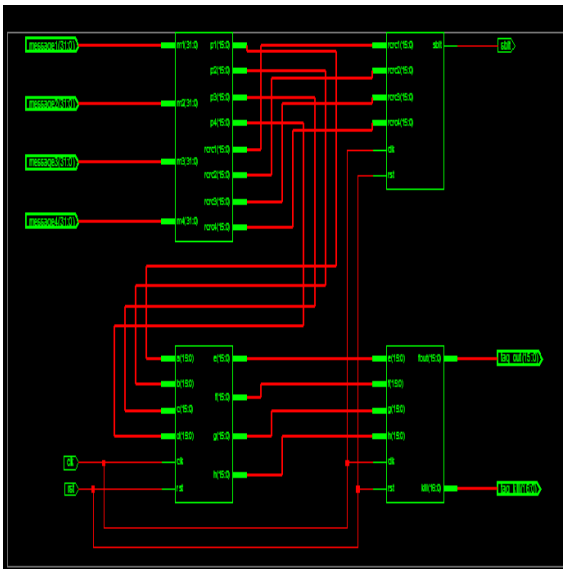
Simulation results of parallel to serial conversion:



Simulation result of prepostrceat module:



RTL Schematic:



4. DEVICE SUMMARY:

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	89	9,312	1%
Number of 4 input LUTs	430	9,312	4%
Logic Distribution			
Number of occupied Slices	222	4,656	4%
Number of Slices containing only related logic	222	222	100%
Number of Slices containing unrelated logic	0	222	0%
Total Number of 4 input LUTs	430	9,312	4%
Number of bonded IOBs	100	232	43%
Number of BUFGMUXs	1	24	4%

5. CONCLUSION

A proposed Reliable and Cost Effective Anti-collision technique (RCEAT) is designed to achieve a reliable and cost effective identification technique of the tag. The RCEAT architecture consists of two main subsystems; PreRCEAT checks error in the incoming packets using the CRC scheme. PostRCEAT identifies the error free packets using Binary Tree based technique. The architecture has been synthesized using Xilinx Synthesis Technology (XST), Simulated using MODELSIM.

6. REFERENCES:

[1] Jhariah, " Reliable and Cost Effective Anti-Collision Technique for RFID UHF Tag"IEEE(2011).

[2] Development and Implementation of RFID Technology, Cristina TURCU.

[3] MIT-AUTOID-TR-003 Efficient Memoryless Protocol for Tag Identification Ching Law, Kayi Lee, and Kai-Yeung Siu fching,kylee,siug@list.mit.edu.

[4] A Practical Parallel CRC Generation Method by Evgeni Stavinov.

[5] "Anti-Collision Algorithm for RFID Tags",Selwyn Piramuthu,Information Systems and Operations Management, University of Florida,

[6] IEEE 802.3 Cyclic Redundancy Check, Author: Chris Borrelli

◈◈◈

EFFICIENT METHOD IN VIDEO STEGNOGRAPHY: USING SECURED DATA TRANSMISSION

[1]K.RAJESWARI, [2]G.V.SRIDHAR & [3]P.N.S. SAILAJA

[1&2]E.C.E department, Al- Ameer College of Engg & IT, Visakhapatnam, India
[3]E.C.E department, Gokul Institute of Tech. & Sci., Bobbili, India

Abstract— Steganography is the art of hiding information in ways that avert the revealing of hiding messages. Video steganography is focused on spatial and transform domain. Spatial domain algorithm directly embedded information in the cover image with no visual changes. This kind of algorithms has the advantage in steganography capacity, but the disadvantage is weak robustness. Transform domain algorithm is embedding the secret information in the transform space. This kind of algorithms has the advantage of good stability, but the disadvantage of small capacity. These kinds of algorithms are vulnerable to steganalysis. This paper proposes a new Compressed Video Steganographic scheme. The data is hidden in the horizontal and the vertical components of the motion vectors. The PSNR value is calculated so that the quality of the video after the data hiding is evaluated.

Index Terms*—Data hiding, least significant bit(LSB), encryption, decryption, PSNR.*

I. INTRODUCTION

A steganography system, in general, is expected to meet three key requirements, namely, imperceptibility of embedding, accurate recovery of embedded information, and large payload (payload is the number of bits that get delivered to the end user at the destination) [1]. In a pure steganography framework, the technique for embedding the message should be unidentified to anyone other than the sender and the receiver. An effective steganography should posses the following characteristics [10-11]:

Secrecy: Extraction of hidden data from the host medium should not be possible without the knowledge of the proper secret key used in the extracting procedure.

Imperceptibility: After embedding the data in the medium, it should be imperceptible from the original medium.

High capacity: The maximum length of the hidden message that can be embedded can be as long as possible.

Resistance: The hidden data should be able to survive when the host medium has been manipulated, for example lossy compression scheme.

Accurate extraction: The extraction of the hidden data from the medium should be accurate and reliable.

This paper explains a way in which so that a video file is used as a host media to hide secret message without affecting the file structure and content of the video file. Because degradation in the quality of the cover object leads to noticeable change in the cover object which may leads to the failure of objective of steganography.

In this paper we consider the motion estimation stage of video compression. The contents are processed during video encoding/decoding. This makes less vulnerable to video steganalysis methods and is lossless coded, thus not prone to quantization distortions. The data bits of the message are hidden in motion vectors. A single bit is hidden in the least significant bit of the each motion vector.

The rest of the paper is organized as follows: in Section II we overview the terms of video compression and decompression. The proposed method is given is explained briefly in Section III and algorithm for our proposed method is given in Section IV followed by the results and analyses in Section V. Finally, the paper is concluded in Section VI.

II. OVERVIEW

In this section, we overview lossy video compression to define our evaluation. There are three types of *pictures* (or frames) used in video compression: I-frames, P-frames, and B-frames centered mainly on amount of data compression. They are different in the following characteristics:

- **I-** (Intra-coded) frames are the least compressible but don't require other video frames to decode.
- **P-** (Predicted) frames use data from previous frames to decompress and are more compressible than I-frames.
- **B-** (Bi-predictive) frames use both previous and forward frames for data reference to get the highest amount of data compression.

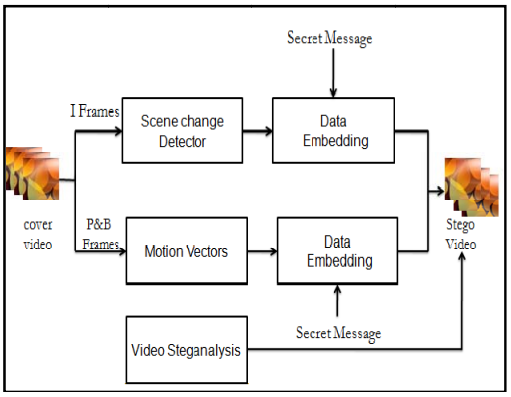


Fig.1: Block diagram of the video stegnograpphy using I, P, B frames separately

At the encoder, the I- frame is encoded using image compression techniques. So the decoder reconstructs it. The I-frame is used as a reference frame for encoding P or B frames. In Motion Picture Expert Group (MPEG-2) standard, the video is ordered into groups of pictures (GOPs) whose frames are encoded in the sequence: [I,B,B,P,B,B,P,B,B]. The temporal redundancy between frames is exploited using block-based motion estimation which is applied on macroblocks B_{ij} of size b b in P or B and searched in target frame(s). The motion field in video compression is translational with horizontal component d^x and vertical component d^y. It's representation in vector form is $d(x)$ for the spatial variables X = ***(x, y)*** in the underlying image. The search window is constrained by assigning limited n-bits for ***d*** i.e.**,** both d^x and $d^y \in [-2^{n-1}, 2^{n-1}-1]$. An exhaustive search in the window of size $b+2^n$ X $b+2^n$ is done to find the optimal motion vector which satisfies the search criterion. Since ***d*** does not represent the true motion in the video, the compensated frame using $(x + \boldsymbol{d(x)})$ is associated with a prediction error $E(x)=(P -)(x)$ in order to be able to reconstruct $P=$ with minimum distortion at the decoder in case of P frame. Similar operation is done for the B-frame but with the average of both the forward compensation from a previous reference frame and backward compensation from a next reference frame. E is of the size of an image and is thus lossy compressed using JPEG compression reducing its data size. The lossy compression quantization stage is a nonlinear process and for every motion estimation method, the pair $(\boldsymbol{d},E)$ will be different and the data size ***D*** of the compressed error will be different. The motion vectors ***d*** are lossless coded and thus become an attractive place to hide a message that can be extracted by a special decoder.

The decoder receives the pair $(\boldsymbol{d},)$, applies motion compensation to form or and decompreses to obtain a reconstructed E_r. Since E and E_r are different by the effect of quantization, then the decoder in unable to reconstruct P identically but it alternatively reconstructs P_r E_r. The reconstruction quality is usually measured by the mean squared error $P - P_r$, represented as peak signal-to-noise ratio (PSNR) and we denote it by R.

III. PROPOSED WORK

A. Video Compression

Video compression uses modern coding techniques to reduce redundancy in video data. Video compression typically operates on square-shaped groups of neighboring pixels, often called macro blocks. These pixel groups or blocks of pixels are compared from one frame to the next and the video compression code sends only the differences within those blocks. In areas of video with more motion, the compression must encode more data to keep up with the larger number of pixels that are changing. Generally, the motion field in video compression is assumed to be translational with horizontal component and vertical component and denoted in vector form by for the spatial variables in the underlying image. Such as three steps search, etc. Administrator chooses one video file along with one key compresses and send to the member. The Authenticated member decompressees the video file and takes the second privacy key.

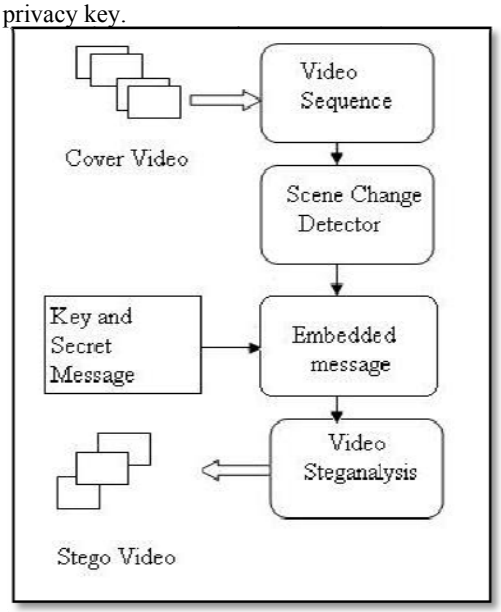


Fig.2: Block diagram proposed model

B. Motion Vector

In video compression, a motion vector is used for motion estimation process. It is used to represent a macro block in a picture. Authenticated person after taking the second privacy key, can see the video in our application, in that video it can detect the motion vector. After seeing this, the member uses the key to see the message sent bu the administrator.

C. Encryption

Encryption is the conversion of data into a form, called a cipher text that cannot be easily understood by unauthorized people. Original message is hidden within a carrier such that the changes occurred in the carrier are not observable. The information about the private key is used to encrypt the text.

D. Extraction of original data

Decryption is the process of converting encrypted data back into its original form, so it can be understood. When the user inputs the correct key that is used at the decryption process, this will extract the original message that is encrypted and embedded.

E. Peak signal-to-Noise Ratio

Larger SNR and PSNR indicate a smaller difference between the original (without noise) and reconstructed image. The main advantage of this measure is ease of computation but it does not reflect perceptual quality. An important property of PSNR is that a slight spatial shift of an image can cause a large numerical distortion but no visual distortion.

IV. ALGORITHM FOR PROPOSED MODEL

Algorithm for Encoding

Step 1: Input cover video file or stream.
Step 2: Read required information of the cover video.
Step 3: Break the video into frames.
Step 4: Compress the frame where the data is to be inserted using any compression technique, DCT was used in this paper.
Step 5: The data was hide using LSB algorithm.

Algorithm for Decoding

Step 1: Input stego video file or stream.
Step 2: Read required information from the stego video.
Step 3: Break the video into frames.
Step 4: Using the motion vector, the frame where the data is hide is chosen.
Step 5: The data is extracted from the LSBs of the identified frame.

V. EXPERIMENTAL RESULTS

Any Steganography technique is characterized mainly by two attributes, imperceptibility and capacity. Imperceptibility means the embedded data must be imperceptible to the observer (perceptual invisibility) and computer analysis (statistical invisibility). The performance of the proposed technique is evaluated using five different video streams (bulb.avi, pearson.avi, plot.avi, sample.avi and sinewave.avi) and one secret data. The perceptual imperceptibility of the embedded data is indicated by comparing the original image or video to its stego counterpart so that their visual differences, if any, can be determined.

Video name	Resolution (W*H)	Frame/Sec.	No. of Frames	size
Bulb	232 X 232	15	80	740KB
Person	356 X 244	15	50	199KB
Plot	560 X 420	15	40	26.9MB
Sample	611 X 352	12	60	555KB
Sine wave	436 X 344	10	101	460KB

Table 1: Cover video file information

Video Name	PSNR (dB)	MSE	Payload (Bytes)	ΔD (Bytes)	ΔR /Frame (dB)
Bulb	38.71	9.51	4439	42014	0.483
Person	37.14	12.55	2545	23267	0.742
Plot	34.07	25.44	3032	27302	0.851
Sample	38.52	9.13	3054	30874	0.642
Sine wave	33.87	26.94	2286	22726	0.335

Table 2: Obtained results information

Additionally, as an objective measure, the Mean squared Error (MSE), Peak Signal to Noise Ratio (PSNR) between the stego frame and its corresponding cover frame are studied. The quantities are given as below.

$$MSE = \frac{1}{H \times w} \sum_{i=1}^{H} (P(i,j) - S(i,j))^2$$

where, MSE is Mean Square error, H and W are height width and P(i,j) represents original frame and S(i,j) represents corresponding stego frame.

$$PSNR = 10 \log_{10} \frac{L^2}{MSE}$$

where, PSNR is peak signal to noise ratio, L is taken as 255.The cover file video details are given in Table 1 and results are tabulated in Table 2.

VI. CONCLUSION

In this paper, we propose and investigate the data hiding method using the motion vector technique for the moving objects, operating directly in compressed domain. This algorithm provides high capacity and imperceptible stego-image for human vision of the hidden secret information. By embedding the data in the moving objects the quality of the video is increased. In this paper, the compressed video is used for the data transmission since it can hold large

volume of the data. The adaptive based compression technique is evaluated such that the data is embedding in the vertical and horizontal component pixels. The PSNR value is calculated to show that the frame is transmitted without any loss or distortion. As a result, the motion vector technique is found as the better solution since it hides the data in the moving objects rather than in the still pictures. The encryption enhances the security of the data being transmitted.

REFERENCES

[1] Hussein A. Aly, "Data Hiding in Motion Vectors of Compressed Video Based on Their Associated Prediction Error", Ieee Transactions On Information Forensics And Security, Vol. 6, No. 1, March 2011

[2] J. Zhang, J. Li, and L. Zhang, "Video watermark technique in motion vector," in *Proc. XIV Symp. Computer Graphics and Image Processing*, Oct. 2001, pp. 179–182.

[3] C. Xu, X. Ping, and T. Zhang, "Steganography in compressed video stream," in *Proc. Int. Conf. Innovative Computing, Information and Control (ICICIC'06)*, 2006, vol. II, pp. 803–806.

[4] P.Wang, Z. Zheng, and J. Ying, "A novel videowatermark technique in motion vectors," in *Int. Conf. Audio, Language and Image Processing (ICALIP)*, Jul. 2008, pp. 1555–1559.

[5] S. K. Kapotas, E. E. Varsaki, and A. N. Skodras, "Data hiding in H.264 encoded video sequences," in *IEEE 9th Workshop on Multimedia Signal Processing (MMSP07)*, Oct. 2007, pp. 373–376.

[6] D.-Y. Fang and L.-W. Chang, "Data hiding for digital video with phase of motion vector," in *Proc. Int. Symp. Circuits and Systems (ISCAS)*, 2006, pp. 1422–1425.

[7] X. He and Z. Luo, "A novel steganographic algorithm based on the motion vector phase," in *Proc. Int. Conf. Comp. Sc. and Software Eng.*, 2008, pp. 822–825.

[8] Mamta Juneja, Parvinder S. Sandhu, and Ekta Walia "Application of LSB Based Steganographic Technique for 8-bit Color Images, World Academy of Science, Engineering and Technology 50 2009 Published

[9] Mritha Ramalingam "Stego Machine – Video Steganography using Modified LSB Algorithm",World Academy of Science, Engineering and Technology 74 2011 Published

[10] Saurabh Singh Invertis University Bareilly, India and Gaurav Agarwal Invertis University Bareilly, India "Hiding image to video: A new approach of LSB replacement", International Journal of Engineering Science and Technology Vol. 2(12), 2010, 6999-7003 Published

[11] JOSEPH GILVARRY School of Computer Applications Dublin City University "Calculation of Motion Using Motion Vectors Extracted from an MPEG Stream" Technical report 20 September 1999 Dublin City University Published

FPGA IMPLEMENTATION OF BUS CONTROL GUARD AND SYSTEM CONTROLLER OF FLEX-RAY CONTROLLER

A. S. KHOBRAGADE & K.M.BOGAWAR

Asistant Professor in Electronics department, Priyadarshini College of Engg, Nagpur,India

Abstract— Flexray is a new communication protocol designed to provide message and complex data exchange between electronic devices installed in a vehicle. The protocol is based on mechanisms in which large bunches of data to be exchanged in real-time and with high dependability between electronic control units This paper gives information about Bus Control Guard and System Controller of the bus guardian module of a flexray controller .Authors have done FPGA Synthesis of the above modules using Xilinx software and shown results on FPGA X3S400 KIT Board.

Keywords-*FPGA; Flexray; BG; X3S400 KIT Board*

I. INTRODUCTION

Flex-ray is a new standard of communication between electronic modules installed in a vehicle. The main target of the new protocol introduction is the growing demand for massive and complex data exchange in the environment where the real time requirement are sometime critical .From topological point of view the flex-ray communication system consists of nodes where each node may be a communication interface of a specific electronic component of a car. According t o t h i s perspective, the Flex Ray protocol, which features data rates up to 10 Mb/s, time and event triggered transmissions, as well as scalable fault-tolerance support was developed and it is now expected to become the future standard for in-vehicle communication.

This paper comprises of eight sections. First three sections discusses a brief overview of the Flex-Ray protocol along with Objective of flex-ray ,flex-ray frame formate and block diagram of a flex-ray communication node. Then the functionality of Bus Guardian is described as a part of communication node. This is followed by the experimental simulation result of two blocks of communication node implemented in VHDL usingmodel sim software .Authors have implemented bus control guard and system controller of flex-ray communication controller on FPGA X3S400 KIT Board.

II. OBJECTIVE OF FLEXRAY

The objective of the FlexRay Consortium has been used to create a communication system for controlling and monitoring applications at different levels :

- At high bit rates, so as to enhance, complement and supplement the applications limited by the bit rate of CAN;
- Capable of implementing X-by-Wire solutions;
- Developing solutions offering redundancy by sending the same messages several times, made possible by the high speed;
- High speed is because of two separate communication channels transmitting the same data in parallel;
- It can also have two communication channels transmitting complementary data in normal time, so as to provide a speed apparently higher than the physical bit rate of the protocol and offering the full use of the remaining channel as a fall-back position;
- Capable of serving all future electronic functions in motor vehicles.
- Flexible system architecture (option to add components)
- Flexible bandwidth, e.g. different rates for control/diagnostic data

III. PROTOCOL OVERVIEW

A. FlexRay Frame Format:

An overview of the Flex Ray frame format is illustrated in Figure 2. The Flex Ray frame is divided into three segments: Header, Payload, and Trailer as :

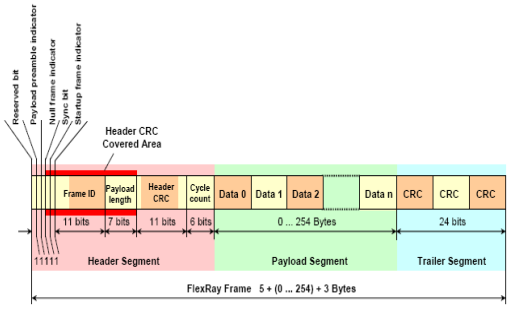


Fig1. Protocol frame structure

a. Header – The Header begins with 5 indicators – the single bits defining basic features of the frame (i.e. whether it is null or synchronizing, or starting, or ordinary data frame). These bits are followed by the 11-bit frame identifier The Frame ID identifies a frame and is used for prioritizing event-triggered frames., then 7-bit frame payload length indicator- The Payload Length contains the number of words which are transferred in the frame., 11-bit CRC protection, covering only selected part of the header and is used to detect errors during the transfer. and 6-bit cycle count indicator--. The Cycle Count contains the value of a counter that advances incrementally each time a Communication Cycle starts.

b. Payload – Payload section contains the main data; its length may be variable, between 0 and 254 bytes. The frame length identifier determines the number of two-byte words in the Payload section.

c.Trailer – Contains three 8-bit CRCs to detect errors.

B. Communications

The Communication Cycle is the fundamental element of the media-access scheme within Flex Ray. Each cycle is a complex structure, containing static segment, dynamic
segment,.

1) Static Segment

The purpose of the static segment is to provide a time window for scheduling a number of time-triggered messages. This part of the Communication Cycle is reserved for the synchronous communication, which guarantees a specified frame latency and jitter through fault-tolerant clock synchronization. The messages which should be transferred in the Static Segment must be configured before starting the communication, and the maximal amount of the data transferred in the Static Segment cannot exceed the duration of the Static Segment

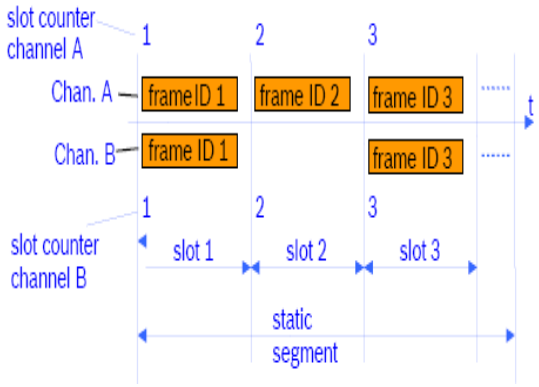


Fig 2.1 Static segment

2) Dynamic Segment

The dynamic segment consisting of minislots (by the macroticks again). This part of cycle may be used for the frames transmission again but the amount of time allotted for a current frame may vary, depending on its length, i.e. Flexible Time Division Multiple Access is applied here. (The authors of FlexRay specification introduce the FTDMA acronym, a bit confusing with the commonly recognized Frequency-Time Division Multiple

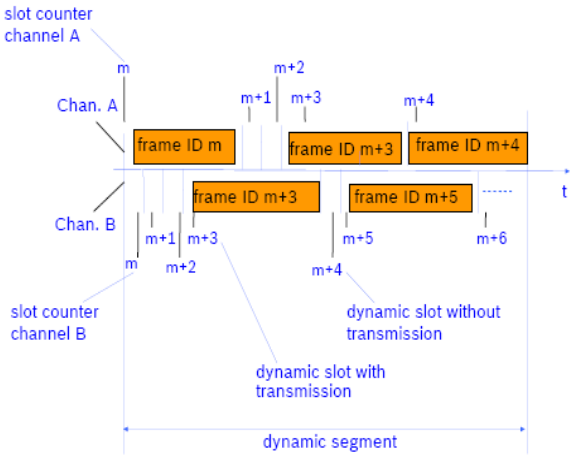


Fig 2.2 Dynamic segment

C. ARCHITECTURE OF THE FLEX-RAY CONTROLLER

Each Flex-Ray node consists of a Host, Communication
Controller, Bus Guardian and Bus Driver

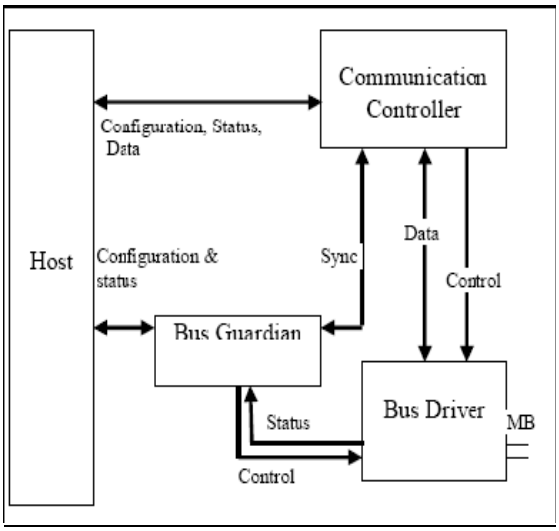


Fig 3. Flex-ray communication controller

D. Architecture of Bus Guardian Module

The bus guardian is used in FlexRay to protect the communication channel against faulty behaviors of communication controllers. Each communication controller has a bus guardian. On the one side, the bus guardian should prevent the communication controller from accessing the communication channel outside its pre-allocated slots. On the other side, the bus guardian should guarantee that messages from non-faulty communication controllers are correctly relayed.

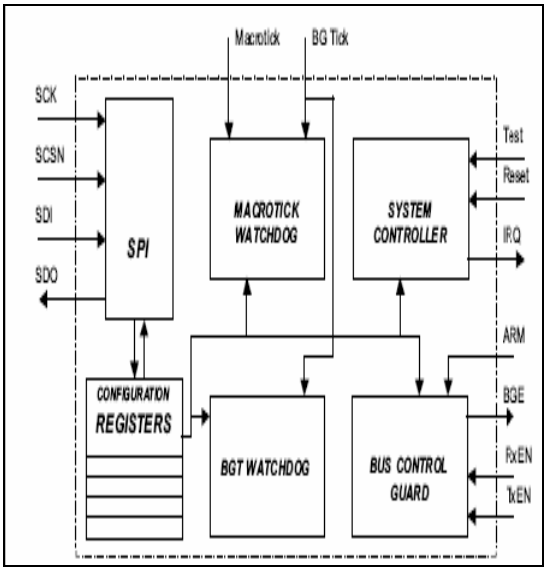


Fig 4 Bock diagram of Bus guardian

The functionality is determined by the:

- Configuration registers, programmed by the software via the serial interface.
- There are two watchdogs detecting anomalous behavior of the synchronization signals.
- Bus Control Guard enables or disables the access to media, depending on ARM and Transmit/Receive enable signals.
- System Controller contains the interrupt controller and two Finite State Machines which determine the current tasks of Bus Guardian.

The block is implemented as a fully synchronous circuit with one clock for all logic, except a small part, counting specific pulses for one of the watchdogs. Bus Guardian operates in 4 modes, represented by the appropriate sates of the FSM.

1) Bus Control Guard .

Bus Control Guard enables or disables the access to media, depending on ARM and Transmit/Receive enable signals.

2) System Controller:

System Controller contains the interrupt controller and two Finite State Machines which determine the current tasks of Bus Guardian.Finite State Machine provides switching between various modes of Bus Guardian operation. There are 4 modes, represented by the appropriate sates of the FSM:

- BG_Fail Silent: In this mode the access to the transmission media is blocked, the node works in this mode after turning the power on and when an error occurs. In the case of error the appropriate interrupts are generated and flags are set. This is also the transition mode between all the others.
- BG_Config: This mode provides read and write access to the registers responsible for configuration of Bus Guardian. The software running on the node host may reconfigure its functionality. This mode may be accessed only after BG_Fail Silent mode, to avoid the risk associated with changes of the configuration when transmission is going.
- BG_WakeUp: Is the special mode when the single node is given permission to wake up the whole set of nodes. This wake up action is made by sending the Wakeup symbols.
- BG_Guarding: Provides the standard operation of the node (i.e. the communication). It may be accessed only from BG_FailSilent mode, usually after successful configuration (made earlier in BG_Config mode) and after the communication schedule was initialised. In the BG_Guarding mode Bus Guardian controls the communication, detecting errors.
-

IV. SIMULATION RESULTS

A. Bus Control Guard

The fig 4. and fig.5 below gives simulation results of Bus Control Guard and System Controller. Accordingly ,in final simulation result we can study different modules status with respect to there assign signals .There are 20 input signal and 3 output signal, with some intermediate signals or processes signals .

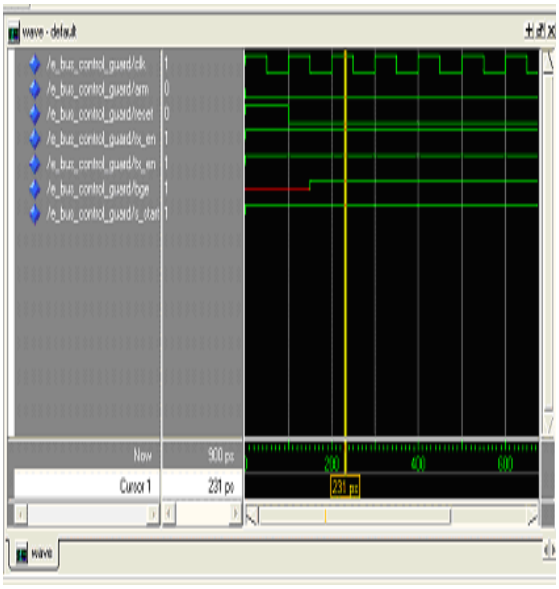


Fig 5 Bus control guard

Figure 5 shows a simulation waveform for Bus Control Guard enables or disables the access to media, depending on ARM and Transmit/Receive enable signals. It has three input signal tx_en, rx_en, ARM and one output signal bge.
When ARM=0, tx_en=1, rx_en=1 then an only then bge=1. This stand fixed assign value is there to perform data transmission and received function.

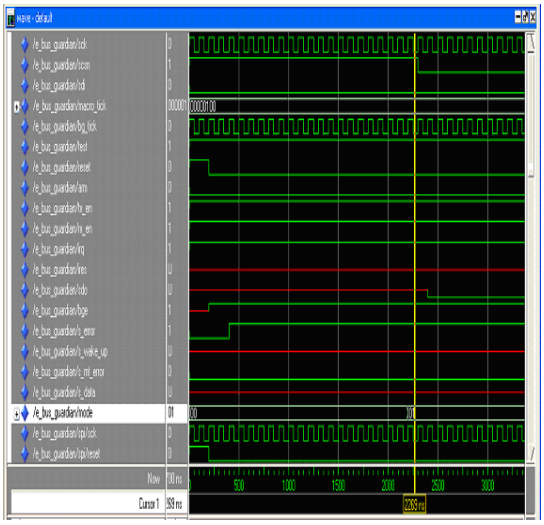


Fig 6. Operation of Bus Control Guard

Figure 6 shows simulation waveform for Bus Control Guard . from this simulation we declare the basic operation of Bus Control Guard. From module architecture point of view when arm=0, tx_en=1 and rx_en=1 as input signals then and only then BGE output signal =1.It also depends upon reset condition ie when reset =1 then it consider as ideal state ,the system becomes reset then when we assign reset=0 then the system starts working and BGE=1.

B. System Controller

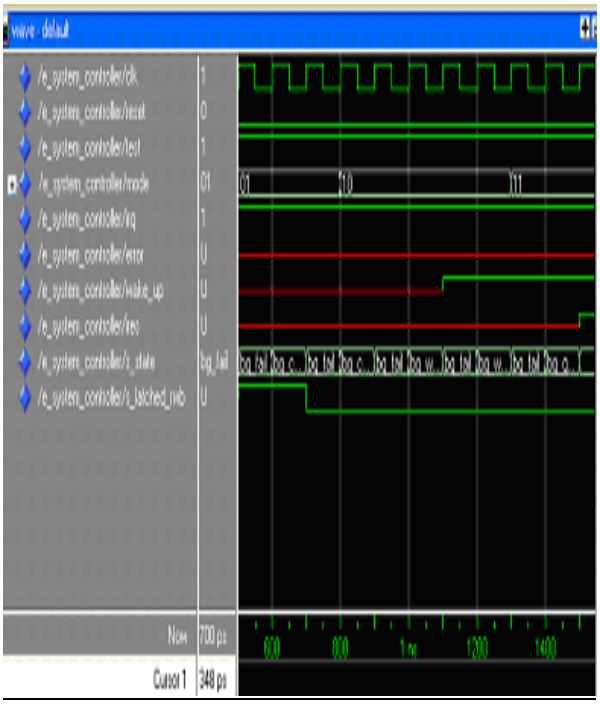


Fig 7 System Controller

Figure 7 shows a simulation waveform for System Controller .System Controller contains the interrupt controller and two Finite State Machines which determine the current tasks of Bus Guardian. Initially assign input signals are clk=1,reset=0,test=1.

*BG_Fail Silent: In this mode the access to the transmission media is blocked, the node works in this mode after turning the power on and when an error occurs. Mode=00 then it perform **ideal operation .**

*BG_Config: This mode provides read and write access to the registers responsible for configuration of Bus Guardian. This mode may be accessed only after BG_Fail Silent mode, to avoid the risk associated with changes of the configuration when transmission is going.when mode=01. then **latchup_rwb=1.**

*BG_WakeUp: Is the special mode when the single node is given permission to wake up the whole set of nodes. This wake up action is made by sending the Wakeup symbols. Whenmode=10 then **wake up=1** which is active high signal.

*BG_Guarding: In the BG_Guarding mode Bus Guardian controls the communication, detecting errors.when mode=11 and when we assign irq=1 then **ires=1.**

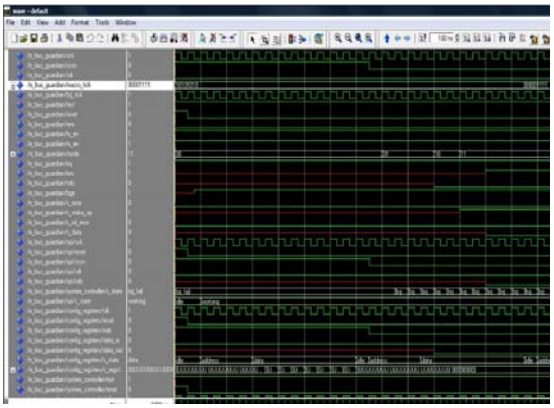


Fig 8 Different modes of System Controller

Figure 8 shows simulation waveform specially for System Controller , it operates in 4 different modes .Initally 2 clocks are applied as sck and bg_tick as a input. System Controller contains the interrupt controller and two Finite State Machines which determine the current tasks of Bus Guardian. Finite State Machine provides switching between various modes of Bus Guardian operation. There are 4 modes, represented by the appropriate sates of the FSM: 00,01,10,11.

V. CODING AND SYNTHHESIS

To check the Functionality of the device, Standard procedures were applied using VHDL. The FPGA synthesis of the circuit was performed with the XILINX software.

VI. CONCLUSION

This paper gives idea about implementation of Bus Control Guard and System Controller of Flex-ray controller using VHDL language on model sim and provide Flex-ray frame format. The concept was try to implemented in VHDL, and synthesized for FPGA .VHDL coding is down loaded into FPGA, which is used for various applications. The Flex-Ray networking standard for motor vehicles provides a foundation that will shape the control structure of automotive electronics for many years It is used in several companies operating in the field of automotive and electronic industry .The study of protocol specification brought serious doubts about the real need for this level of complexity The reason could be too strong requirements for the protocol flexibility The mixture of TDMA and FDMA applied in the same kind of communication cycle which provided flexibility and diversity of solutions.

On the other hand in spite of the functional Further,the concept which was implemented in VHDL, try to verify and successfully synthesized in FPGA. Selected details of the design were presented. From authors point of view it was one more step in the extensive study of various communication protocols. Simulation of the basic functionality of the other devices, coupled with Bus Guardian was written in VHDL, We cover all the possible working conditions, would require the effort, significantly to exceed the project itself.

VII. REFERENCES

[1]. "On Hardware implementation of flex-ray bus guardian module", Proc. 12th MIXDES JUNE 2007. Flex-Ray Communications System – Protocol Specification, v2.0, Flex-Ray Consortium, June 2004

[2]. Flex-Ray Communications System – Electrical Physical Layer Specification, v2.0, Flex-Ray Consortium, June 2004.

[3]. Flex-Ray Communications System - Bus Guardian Specification, v2.0, Flex-Ray Consortium, June 2004.

[4]. ATMega 8535, technical specification, ATMEL 2005.

[5]. IEEE Standard VHDL Language Reference Manual, (IEEE Std 1076), 2000 Edition.

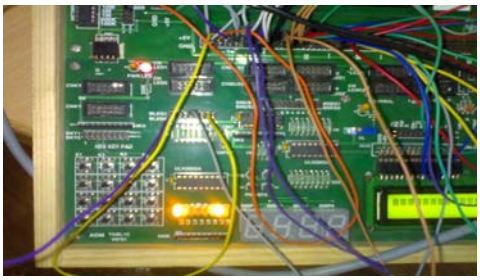
[6]. IEEE 1164 Standard Multivalue Logic System for VHDL Model Interoperability (Std_Logic_1164), (IEEE Std 1164), 1993 Edition.

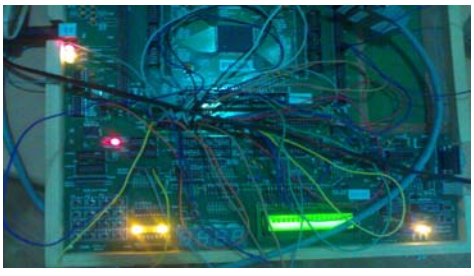
[7]. Introduction to Quartus II, Altera Corporation, San Jose, 2003.

[8]. P.M. Szecówka, P. Wasilko, SONET/SDH frame transmitter implementation in digital IC, Proc. 11th, MIXDES, 2004, pp 258-262.

[9]. P.M. Szecówka, M.Burski, ATM transmission controller implementation in digital IC, Proc. 12th MIXDES 2005, pp 61-64.

[10]. P.M. Szecówka, A. Kara , Hardware support for the digital video broadcast bitstream extraction, Proc. 12th MIXDES, 2005, pp 137.





◈◈◈

POWER QUALITY IMPROVE OF NETWORK AND LOADS BY USING OPEN UPQC

S.CHAITHANYA , O.HEMAKESAVULU & M. PADMA LALITHA

Department of Electrical Engg, P.G Student, AITS College, Rajampeta,

Abstract- Power quality (PQ) is very important to certain customers. For this reason, many utilities could sell electrical energy at different prices to their customers, depending on the quality of the delivered electric power. Since most end users are connected to secondary. Currently, the quality of supplied power is important to several customers. Power quality (PQ) is a service and many customers are ready to pay for it. In the future, distribution system operators could decide, or could be obliged by authorities, to supply their customers with different PQ levels and at different prices. A new device that can fulfill this role is the OPEN unified power quality conditioner (UPQC), composed of a power-electronic series main unit installed in the medium-voltage/low-voltage (LV) substation, along with several power-electronic shunt units connected close to the end users. The unified power quality conditioner (UPQC) compensator seems to be a particularly promising power conditioner device. This apparatus is constituted of a series and a shunt unit, with a common dc section through which power can be exchanged. Its function is to improve the quality levels of the current absorbed at the mains and the load supply voltage. However, these devices do not allow local distributors to guarantee different quality demand levels to the final ustomers, because they improve power quality for all the supplied end users. The installation investments are also quite high relative to the power quality level obtained. A solution that has similar performances and advantages, but also makes cost reduction possible, is the proposed OPEN UPQC .The series and parallel units do not have a common dc link, so their control strategies are different than traditional UPQC control techniques. This device can achieve general improvement in PQ, reducing the most common disturbances for all customers that are supplied by the mains (PQ) by using only the series unit. Additional increments in PQ (i.e., mains power interruptions), can be provided to the customers who need it (custom power) by the shunt units. Therefore, this new solution combines an improvement in PQ for all end users, with a cost reduction for those that need high quality power. The proposed solution has been analyzed and described, and a model of a 400-kVA LV grid is considered a test network to evaluate the steady-state performance and functioning limits. The results obtained under steady-state conditions justify the configuration chosen and good device performance. The OPEN UPQC apparatus is a good compensation system if wide installation of shunt units is needed. An increase in the percentage of the protected load enhances the voltage stabilization interval over which the OPEN UPQC can significantly improve the power quality, especially if the load power factor takes a high value. So, MATLAB/SIMULINK software tool was used to simulate and for the study of this system.

I. INTRODUCTION

Power quality (PQ) is a service and many customers are ready to pay for it. In the future, distribution system operators could decide, or could be obliged by authorities, to supply their customers with different PQ levels and at different prices. A new device that can fulfill this role is the OPEN unified power quality conditioner (UPQC), composed of a power-electronic series main unit installed in the medium-voltage/low-voltage (LV) substation, along with several power-electronic shunt units connected close to the end users. The series and parallel units do not have a common dc link, so their control strategies are different than traditional UPQC control techniques. This device can achieve general improvement in PQ, reducing the most common disturbances for all customers that are supplied by the mains (PQ) by using only the series unit. Additional increments in PQ (i.e., mains power interruptions), can be provided to the customers who need it (custom power) by the shunt units. Therefore, this new solution combines an improvement in PQ for all end users, with a cost reduction for those that need high quality power. The proposed solution has been analyzed and described, and a model of a 400kVA LV grid is considered a test network to evaluate the steady-state performance and functioning limits. The results obtained under steady-state conditions justify the configuration chosen and good device performance. The OPEN UPQC apparatus is a good compensation system if wide installation of shunt units is needed. An increase in the percentage of the protected load enhances the voltage stabilization interval over which the OPEN UPQC can significantly improve the power quality, especially if the load power factor takes a high value.

II. POWER QUALITY ISSUES

The contemporary container crane industry, like many other industry segments, is often enamored by the bells and whistles, colorful diagnostic displays, high speed performance, and levels of automation that can be achieved. Although these features and their indirectly related computer based enhancements are key issues to an efficient terminal operation, we must not forget the foundation upon which we are building. Power quality is the mortar which bonds the foundation blocks. Power quality also affects terminal operating economics, crane reliability, our environment, and initial investment in power distribution systems to support new crane installations.

A. POWER QUALITY:

Power quality (PQ) is a service and many customers are ready to pay for it. It is very important to certain customers. For this reason, many utilities could sell electrical energy at different prices to their customers, depending on the quality of the delivered electric power. Since most end users are connected to secondary. Currently, the quality of supplied power is important to several customers. In the future, distribution system operators could decide, or could be obliged by authorities, to supply their customers with different PQ levels and at different prices. There are some power quality problems are,

I. SAGS:

One of the most common power quality problems today is voltage dips. Voltage sags (dips) are short-duration reductions in rms voltage caused by short-duration increases of the current, typically at another location than where the voltage sag is measured. The most common causes of over currents leading to voltage sags are motor starting, transformer energizing and faults. Also capacitor energizing and switching of electronic load lead to short duration over currents, but the duration of the over current is too short to cause a significant reduction in the rms voltage. These events are normally not referred to as voltage sags but as voltage notches or voltage transients. Voltage sags due to short circuit and earth faults are the cause of the vast majority of equipment problems. Most of the recent emphasis on voltage sags is directed towards these fault-related sags.

II. SWELLS:

Swell is an RMS increase in the AC Voltage, at the power frequency, for duration from a half a cycle to a few seconds. Voltage can rise above normal level for several cycles to seconds. When single phasing occurs, a loss of one of three energized conductors, an imbalance in the two remaining energized conductors will result where a voltage increase can be experienced; sudden decrease in line loads; re-energizing of power after a utility power interruption, when power comes back in; open neutrals; loose wiring. Voltage swells can originate internally in building wiring or externally on power lines. Voltage swells are the least frequent of the power line problems representing only about 2 to 3% of all power problems occurring to industry studies. Voltage swells will normally cause damage to lighting, motor and electronic loads and will also cause shutdown to equipment. With electronically controlled equipment, voltage above 6 to 10% above normal may result in damage.

III. CUSTOM POWER DEVICES

The basic applications of FACTS-devices are Power flow control, Increase of transmission capability, Voltage control, Reactive power compensation, Stability improvement, Power quality improvement, Power conditioning, Flicker mitigation, Interconnection of renewable and distributed generation and storages. The usage of lines for active power transmission should be ideally up to the thermal limits. Voltage and stability limits shall be shifted with the means of the several different FACTS devices. It can be seen that with growing line length, the opportunity for FACTS devices gets more and more important. The compensating devices either compensate a load, i.e., correct its power factor, unbalance etc. or improve the quality of the supplied voltage. These devices are either connected in shunt or in series or combination of both. The devices include:

1) Active Power Filters
2) Dynamic Voltage Restorer (DVR)
3) Distributed statcom (D-statcom)
4) Unified Power Quality Conditioner (UPQC)

A. ACTIVE POWER FILTERS:

The increasing use of power electronics based loads (adjustable speed drives, switch mode power supplies, etc.) to improve system efficiency and controllability is increasing the concern for harmonic distortion levels in end use facilities and on the overall power system. The application of passive tuned filters creates new system resonances which are dependent on specific system conditions. In general, passive tuned filters have been used to minimize low-frequency current harmonics while high-pass units have been connected to attenuate the amplitude of high frequency current components. However, high-pass filters present disadvantages due to the resistance connected in parallel to the inductor, which increases the filter losses and reduces the filtering effectiveness at the tuned frequency. The most critical aspects of passive filters are related to the fact that they cannot modify their compensation characteristics following the dynamic changes of the nonlinear load, the performance dependence they present with the power system parameters, and the probability of series resonances with the power system's equivalent reactance. Another technical disadvantage of passive filters is related to the small design tolerances acceptable in the values of L and C. Small changes in the value of L or C modify the filter resonant frequency. For example, a 5% difference in the selected value of L or C in a second-order LC filter tuned at 250 Hz (fifth harmonic) modifies the required resonant frequency in 7% with respect to the selected design value, affecting the filter current harmonic compensation performance. Also, the passive filter generates at fundamental frequency reactive power that changes the system voltage

regulation, and if the filter is not designed properly or disconnected during low load operating conditions, over voltages can be generated at its terminals.

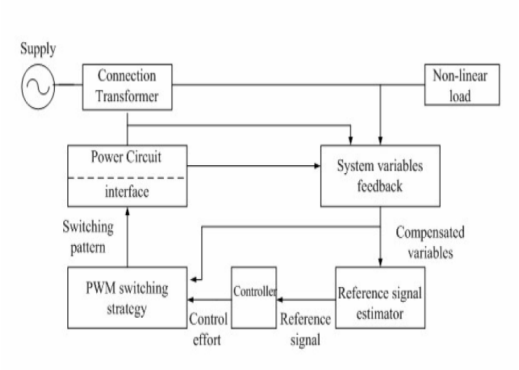


Figure 3.1 Generalized block diagram for active power filter.

B. DYNAMIC VOLTAGE RESTORER (DVR):

The DVR is a powerful controller that is commonly used for voltage sags mitigation at the point of connection. The DVR employs the same blocks as the D-STATCOM, but in this application the coupling transformer is connected in series with the ac system, as illustrated in Fig. 3.2. The DVR is a distribution voltage solid-state DC-to-AC switching converter that injects three single-phase AC output voltages in series with the distribution feeder and in synchronism with the voltages of the distribution system. By injecting voltages of controllable amplitude, phase angle, and frequency (harmonic) into the distribution feeder in instantaneous real time via a series-injection transformer, the DVR can "restore" the quality of voltage at its load-side terminals when the quality of the source-side terminal.

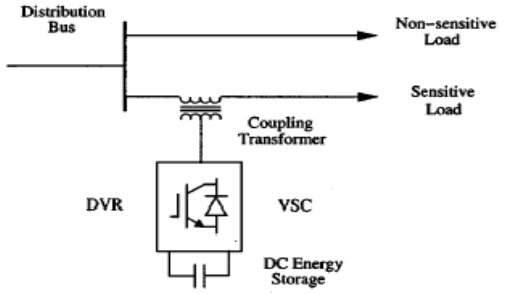


Fig 3.2 Schematic representation of a DVR for a typical custom power application.

C. D-STATCOM:

It is the equivalent to the STATCOM in the distribution level. In its most basic form, the D-STATCOM configuration consists of a two-level VSC, a DC energy storage device; a coupling transformer connected in shunt with the ac system, and associated control circuits. More sophisticated configurations use multi pulse and/or multilevel configurations. Figure 3.3 shows the schematic representation of the D-STATCOM.

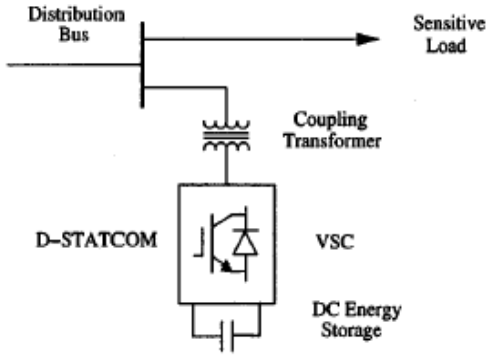


Fig 3.3: Schematic representation of the D-STATCOM as a custom power controller

The VSC converts the DC voltage across the storage device into a set of three-phase AC output voltages. These voltages are in phase and coupled with the ac system through the reactance of the coupling transformer. Suitable adjustment of the phase and magnitude of the D-STATCOM output voltages allows effective control of active and reactive power exchanges between the D-STATCOM and the ac system. The VSC connected in shunt with the ac system provides a multifunctional topology which can be used for up to three quite distinct purposes:

- Voltage regulation and compensation of reactive power;
- Correction of power factor;
- Elimination of current harmonics.

The design approach of the control system determines the priorities and functions developed in each case. In this figure, the D-STATCOM is used to regulate voltage at the point of connection. The control is based on sinusoidal PWM and only requires the measurement of the rms voltage at the load point.

D. UNIFIED POWER QUALITY CONDITIONER:

The provision of both DSTATCOM and DVR can control the power quality of the source current and the load bus voltage. In addition, if the DVR and STATCOM are connected on the DC side, the DC bus voltage can be regulated by the shunt connected DSTATCOM while the DVR supplies the required energy to the load in case of the transient disturbances in source voltage. The configuration of such a device (termed as Unified Power Quality Conditioner (UPQC)) is shown in Fig. 3.4. This is a versatile device similar to a UPFC. However, the control objectives of a UPQC are quite different from that of a UPFC.

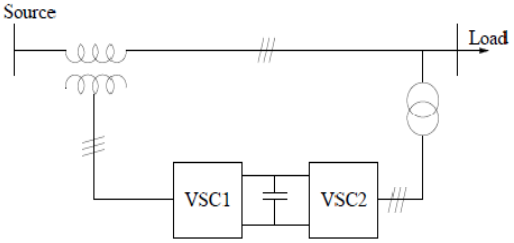


Fig3.4: unified power quality conditioner.

The shunt connected converter has the following control objectives:

1. To balance the source currents by injecting negative and zero sequence components required by the load
2. The compensate for the harmonics in the load current by injecting the required harmonic currents
3. To control the power factor by injecting the required reactive current (at fundamental frequency)
4. To regulate the DC bus voltage.

The series connected converter has the following control objectives:

1. To balance the voltages at the load bus by injecting negative and zero sequence voltages to compensate for those present in the source.
2. To isolate the load bus from harmonics present in the source voltages, by injecting the harmonic voltages
3. To regulate the magnitude of the load bus voltage by injecting the required active and reactive components (at fundamental frequency) depending on the power factor on the source side
4. To control the power factor at the input port of the UPQC (where the source is connected. Note that the power factor at the output port of the UPQC (connected to the load) is controlled by the shunt converter.

IV. MODELLING OF OUPQC

Most end user disturbances are characterized by short duration and small amplitude, though they can still cause interruptions in production processes. Most voltage sags have small depth and short durations. More than 95% of voltage sags can be compensated by injecting a voltage of up to 60% of the nominal voltage, with a maximum duration of 30 cycles. This information is primarily used to evaluate a suitable size for the OPEN UPQC.

A.THE OPEN UPQC

The series unit of the OPEN UPQC, sized to supply 60% of the LV network power and equipped with a small storage system, can compensate for most of the voltage disturbances.

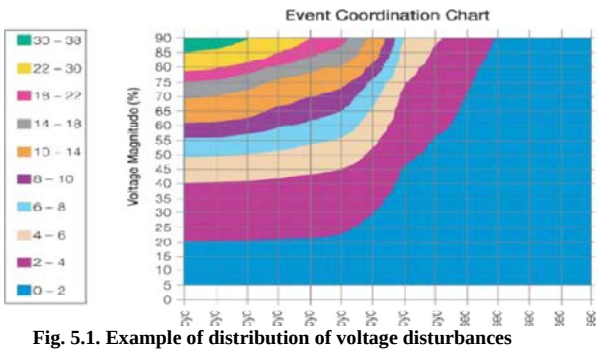


Fig. 5.1. Example of distribution of voltage disturbances reported in the EPRI event coordination chart

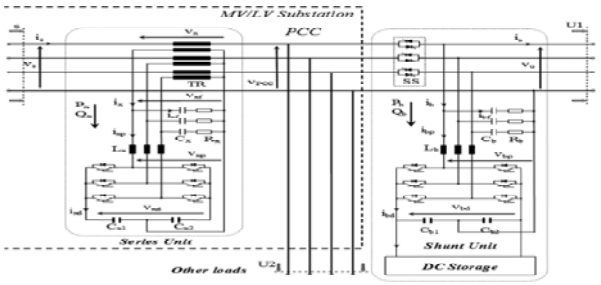


Fig. 5.2. Multiwire power diagram of the new proposed solution. The shunt units consist of an ac/dc power converter, similar to the one used in the series unit, connected to an energy storage system and a set of static switches (SS). The shunt unit, depending on the state of the network voltage, can supply either the entire load, or a part of the load. There are two different modes of OPEN UPQC operation:

- **COMPENSATOR:** when the PCC voltage is within its operation limits, the SS are closed, the series unit works as a three phase voltage generator and the shunt units work as current generators.

- **BACK-UP**: when the PCC voltage is outside of its operation limits, the SS are open, decoupling the network and the load-compensator system. Each sensitive load is supplied by its shunt unit, which acts as a sinusoidal voltage generator, using the energy stored in the storage system as an energy source.

B. OPEN UPQC PERFORMANCE:

This section is focused on understanding the OPEN UPQC compensation limits. The analysis will be carried out under steady state conditions, to evaluate the compensation capacity of the device in normal operation mode $0.9V_n \le V_s \le 1.1V_n$. It is important to remember that the power absorbed by the loads and the shunt units influences the performance of the series unit, and therefore of the whole OPEN UPQC.

Therefore, when considering a particular set of load conditions, it is possible to find operating conditions for the shunt units that increase the compensating limits of the series unit. Depending on whether or not storage systems are present, the series and shunt units can exchange only non active power or both non active power and active power with the mains. In the latter case, as will be shown in the following, the OPEN UPQC can better compensate for short duration disturbances. In the following case, all of the solutions will be analyzed under the assumption that the voltages are sinusoidal and are constituted of only the positive sequence component in the different network buses. It is important to emphasize that suitably coordinating the various units of the OPEN UPQC allows for a wide compensation range, comparable with the UPS, but more economical. This coordination requires a communication system (i.e., based on the carrier waves) between the series unit and the shunt units, but this system cannot be very fast. Moreover, in transient analysis, the communication between the series unit and the shunt units cannot be included (the communication could be slow, could be out of order, etc.).. Therefore, each unit Necessarily works alone The angle can be calculated by the equation shown at the bottom of the page.

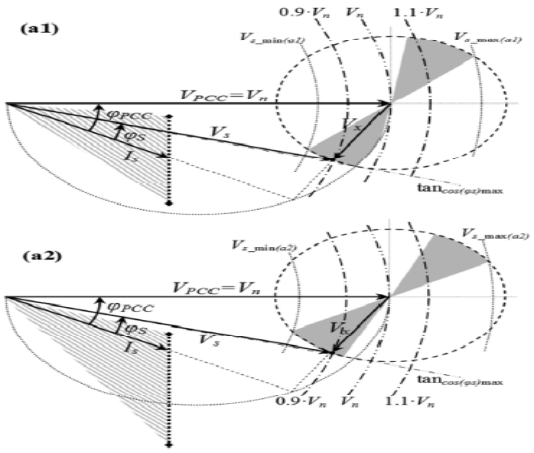


Fig. 5.3. Voltage compensation, exchanging only nonnative power. Case (a1): it is possible to obtain a power factor equal to 1 in s section in low-voltage situations. Case (a2): the power factor always less than one.

C.NONACTIVE AND POWER EXCHANGE

The conditions under which all of the converters exchange only non active power must be confirmed in situations when the system voltage Vs is near the contractual limits (normal operation mode). In normal operation mode, the maximum voltage drop in the LV lines of the network must be less than 5% to maintain low power loss. Therefore, if all the converter units are operating to stabilize the voltage in the PCC at its nominal value (100%), the load voltage value will be at least 95% of the nominal voltage. This result allows an improvement of one of the aspects of the supply quality, the stability of the real value of the supply voltage, for all customers. Therefore, the OPEN UPQC works to stabilize the nominal voltage at the PCC. The phasor diagram of the OPEN UPQC is shown in Fig 5.3.In order to avoid active power injections, the series voltage V_x has to be in quadrature with the mains current I_s. The V_x vaue is reported in (5.1)

$$\overline{V_x} = \overline{V}_{pcc} . \frac{\sin(\varphi_{cc} - \varphi_s)}{\cos(\varphi_s)}$$

…(5.1)

The current Is is primarily composed of the current of unprotected loads Us (whose phase difference with respect to V_{pcc} cannot be varied) and the current of protected loads (whose phase difference with respect to V_{pcc} can be changed by the shunt units) as reported in (5.2), where Pu1,2 and Qu1,2 are the active and reactive power of the equivalent load respectively, P_{losses} and Q_{losses} are the active and reactive power lines losses, respectively, and Q_b is the reactive power injected by all the shunt units

$$I_s = \frac{P_{u1} + P_{u2} + P_{losses} + j.(Q_{u1} + Q_b + Q_{losses})}{V_{pcc}}$$

…(5.2)

Therefore, the angle φ_{pcc} can oscillate between the upper and lower limits φ_{pcc_max} and φ_{pcc_min}, obtained when $Q_b = A_1$ and $Q_b = -A_1$ respectively, in the area highlighted in Fig. 5.3. The angle can be calculated by the equation shown as

$$Cos(\varphi_{pcc}) = \frac{P_{U1} + P_{U2} + P_{losses}}{\sqrt{(P_{U1} + P_{U2} + P_{losses})^2 + (Q_{U1} + Q_{U2} + Q_b + Q_{losses})^2}}$$

…(5.3)

The quantities V_{s_max} and V_{s_min} can be obtained with eq (5.4) and(5.5)

$$V_{s\_max} = V_{x\_max}{}^2 + V_{pcc}{}^2 + 2.V_{pcc}.V_{x\_max}.Sin(\varphi_{pcc\_max})$$

…(5.4)

$$V_{s\_min} = V_{x\_max}{}^2 + V_{pcc}{}^2 + 2.V_{pcc}.V_{x\_max}.Sin(\varphi_{pcc\_max})$$

…(5.5)

The current phasor I_a can move along the black dotted line, varying the reactive power Q_b of the shunt units. In case (a1) in particular, it is possible to obtain a power factor equal to 1 in the section in low voltage situations, because the line $\tan\cos(\phi_s)\max$ intercepts the black dotted line. In case (a2), the power factor is always less than 1.

Assuming that, the range $V_{s\_\max} + V_{s\_\min} \approx 2.V_{pcc}$, the range amplitude $V_{s\_\max} - V_{s\_\min}$ can be obtained with

$$V_{s\_\max} - V_{s\_\min} \approx 2.V_{s\_\max}.\sin(\varphi_{pcc\_\max}) \quad \ldots(5.6)$$

V. SIMULATION RESULTS

In this project, the OPEN UPQC is tested under the different types of disturbances such as voltage sags and interruption occurred on a preferred distribution system. The proposed work is carried out using MATLAB/SIMULINK. Simulation results are presented and analyzed. The voltage vectors which are generated by the sub system in the DVR is show in Fig 5.1.

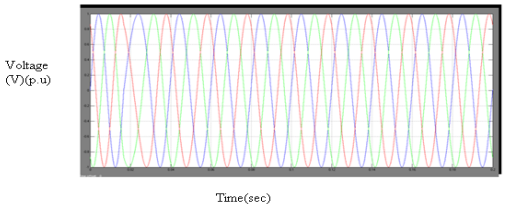


Fig.5.1 Voltage vectors

The series voltage is shown in Fig.5.2.

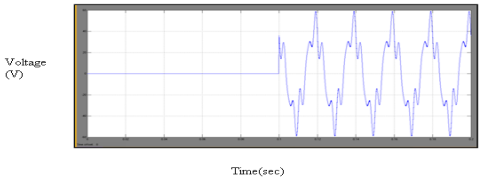


Fig. 5.2 Series voltage

The load voltage which is obtained in the distribution system when the voltage sag occurs is shown in Fig.5.3.

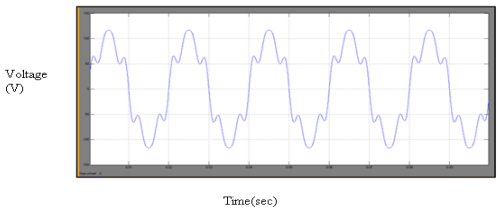


Fig.5.3 Load voltage

The load voltage of the distribution system when the device OUPQC is in operation condition is shown in Fig. 5.4.

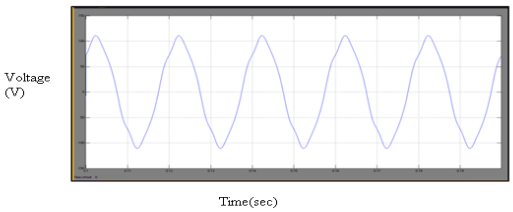


Fig.5.4 load voltage

The DC voltage is show in Fig.5.5.

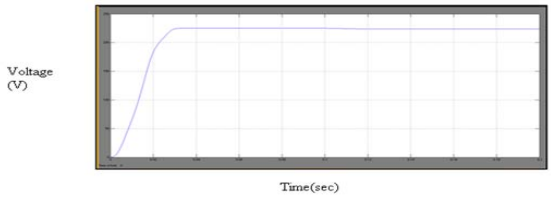


Fig.5.5 DC voltage

The load current when the disturbances occurred in the system Fig.5.6.

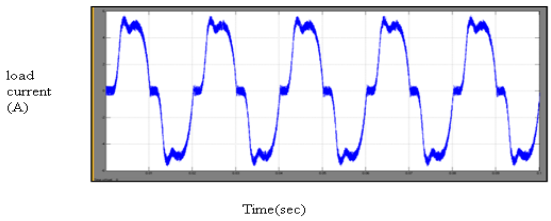


Fig. 5.6 Load current

The load current when the disturbances are removed in the distribution system is shown in Fig.5.7.

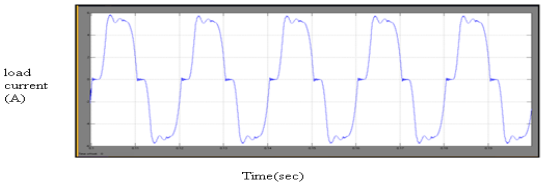


Fig. 5.7 load current

The power factor of the distribution system is shown in Fig.5.8.

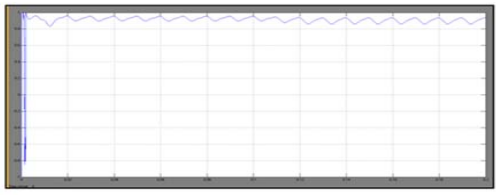


Fig.5.8 power factor

VI. CONCLUSION

The OPEN UPQC apparatus is a good compensation system if wide installation of shunt units is needed. An increase in the percentage of the protected load enhances the voltage stabilization interval over which the OPEN UPQC can significantly improve the power quality, especially if the load power factor takes a high value. If the power factor of load is less than one, the power factor in section increases, to avoid nonnative power absorption from the mains. For low values of the parameter, the OPEN UPQC becomes expensive if there are few shunt units. In this case, it is better to install other compensation device typologies (as UPS, UPQC, etc.) near the sensitive loads, and a nonnative compensator system near the non-sensitive loads if necessary. It is possible to conclude that installation of the series unit is a cost-effective way for distributors to improve the power quality level in the distribution networks in order to achieve the standards imposed by the authorities. Compensation improvement for the sensitive end users can be achieved by installing a shunt unit near them, instead of the more expensive UPS device. At this moment, the OPEN UPQC study is still under investigation. The dynamic behavior, considering changing operating modes, of a 5 kW prototype shunt unit is developed and experimental results are presented. The large investments are needed to analyze the completed solution, and availability of electrical distribution operators for an infield test will be required. Number of installations of Custom Power Devices is increasing in the world. Increasing competitiveness and new utility regulations force the industrial consumers towards installation of Custom Power Devices. Mostly shunt active power filter installations are reported in the market and research on Custom Power Devices is expected to grow in the near future.

REFERENCES:

[1] Morris Brenna, Roberto Faranda, Enrico Tironi, "A New proposal for power quality and custom power improvement:OPENUPQC,"IEEETans.PowerDelivery.,vol.24,no.4,oct.2009.

[2] D. M. Divan, W. E. Brumsickle, G. A. Luckjiff, J. W. Freeborg, and R. L. Hayes, "Realizing a nation-wide power quality and reliability monitoring system," 2003. [Online].Available:http://www.softswitch.com/docs/Realizing%20a%20Nationwide%20System%202003.pdf.

[3] B.Wang, G. Venkataramanan, and M. Illindala, "Operation and control of a dynamic voltage restorer using transformer coupled H-bridge converters," IEEE Trans. Power. Electron., vol. 21, no. 4, pp. 1053–1061, Jul. 2006.

[4] D. M. Vilathgamuwa, H. M. Wijekoon, and S. S. Choi, "A novel technique to compensate voltage sags in multiline distribution system—The interline dynamic voltage restorer," IEEE Trans. Ind. Electron., vol. 53, no. 5, pp. 1603–1611, Oct. 2006.]

[5] C. N. M. Ho and H. S. H. Chung, "Fast transient control of singlephase Dynamic Voltage Restorer (DVR) without external DC source," in Proc. 37th IEEE Power Electronics Specialists Conf., Jeju, Korea, Jun. 18–22, 2006, pp. 2105–2111.

[6] K.R. Padiyar "Facts controllers in power transmission and distribution", NEW AGE INTERNATIONAL (P) LIMITED, PUBLISHERS, 2007

[7] A. Ghosh and G. Ledwich, "Compensation of distribution system voltage using DVR," IEEE Trans. Power Del., vol. 17, no. 4, pp. 1030–1036, Oct. 2002.

[8] M. K. Mishra, K. Karthikeyan, and P. K. Linash, "A development and implementation of DSP based DSTATCOM to compensate unbalanced nonlinear loads," presented at the IEEE Power India Conf., New Delhi, India, Apr. 10–12, 2006.

S.Chaithanya was born in mydukur, A.P, India. He received the B.Tech (Electrical and Electronics Engineering) degree from the vaagdevi engineering college, proddatur in 2010: and Pursuing M.Tech (Electrical Power Systems) from the Annamacharya Institute of Technology and Science , rajampeta.
e-mail: seethachaithu@gmail.com

O.Hemakesavulu was born in Kadapa, A.P, India. He received M.Tech (Power Electronics) degree from Rajeev Gadhi Memorial College of Engineering & Technology, Nandyal And BTech (Electrical and Electronics Engineering) from Annamacharya Institute of Technology and Sciences,Rajampet.Presently pursuing Ph.D. e-mail: hkesavulu 6@gmail.com

M. Padma Lalitha. is awarded Ph.D for her work "Soft Computing Techniques for optimal DG placement in Radial Distribution System " from S.V.U. in the year 2011and is a graduate from JNTU, Anathapur in Electrical & Electronics Engineering in the year 1994. Obtained Post graduate degree in PSOC from S.V.U, Tirupathi in the year 2002. Having 14 years of experience in teaching in graduate and post graduate level. Presently working as Professor and HOD of EEE department in AITS, Rajampet
e-mail: padmalaitha_mareddy @yahoo.co.in

◈◈◈

ON-LINE INTERACTIVE DATA ACQUISITION AND CONTROL SYSTEM

SHAIK.RAKHIL & CH.SIVA RAM

Dept of ECE, Audisankara College Of Engineering and Technology, Gudur, India

Abstract – Design of on-line embedded web server is a challenging part of many embedded and real time data acquisition and control system applications. The World Wide Web is a global system of interconnected computer networks that use the standard Internet Protocol Suite (TCP/IP) to serve billion of users worldwide and allows the user to interface many real time embedded applications like data acquisition, Industrial automations and safety measures etc,. This paper approached towards the design and development of on-line Interactive Data Acquisition and Control System (IDACS) using RM based embedded web server. It can be a network, intelligent and digital distributed control system. Single chip IDACS method improves the processing capability of a system and overcomes the problem of poor real time and reliability. This system uses Atmega8 Processor portability with Real Time Linux operating system (RTLinux RTOS) it makes the system more real time and handling various processes based on multi tasking and reliable scheduling mechanisms. Web server application is ported into an processor using embedded 'C' language. Web pages are written by Hyper text markup language (HTML); it is beneficial for real time IDACS, Mission critical applications, ATM networks and more.

Keywords *- Embedded Atmega8 controller, Real Time Linux Operating system (RTLinux RTOS), Embedded web server, Inte ractive data acquisition and control system (IDACS).*

I. INTRODUCTION

Online Interactive Data Acquisition and Control system plays the major role in the rapid development of the fast popularization and control in the field of measurement and control systems. It has been designed with the help of many electrical, electronic and high voltage equipments; it makes the system more complicated and not reliable. This paper approaches a new system that contains inbuilt Data Acquisition and Control system DACS) with on-line interaction. It makes the system more reliable and avoids more complication. It is the great demand in consumer applications and many industries. The design of very fast data acquisition in plasma discharge application was discussed in [1]; this system replaces various complex cables which are used for acquisition and it uses FPGA and ARM processor for data acquisition and digital diagnosis. There are various digital DAC systems are available for the substitution of multisite job operation. A single worker can interact with the machine and collect various data from on- going work in a single work station. The simplest design of data acquisition system is detailed in [2], which is based on Linux Operating system [3]; it is the popular choice for many embedded real time applications and PC systems. The design of flexible and networked data acquisition architecture was approached in [4], where the software resources are stored in local memory to avoid the level of resource usage and increases system's efficiency. This system process the client based on dynamic manner by server response and it maintains separate data base with DAC controller. In [5] advanced traffic survey mechanism uses data collection process for post processing of vehicle's position. Signal conditioning is the major part of any data acquisition unit. High level integration architecture was discussed in [6]; it allows signals to be conditioned, simultaneously acquired according to the external clock and triggers processed and transferred data to real time servers. Signal measurement from astrophysical sources is described in [7]; where the shared memory and internet protocols are used for data handling and process from remote users. It was developed with Global Positioning System (GPS) and Environmental monitoring system. Similarly depends on industry and its location General Packet Radio Service (GPRS) also used for data transmission through on-line. But this paper doesn't use GPRS and GPS systems for data uploading into internet. It reduces the system complexity and effective for all kind of real time applications. Every real time embedded system should be run by real time operating systems. Even a small 8-bit microcontroller has the portability with RTOS is developed in [8]. In this paper Real time Linux Operating system is ported in ARM9 processor. Generally all ARM9 processors have the

portability with any kind of higher end RTOSes. This RTLinux RTOS is very effective for many embedded applications [9] & [10]. Here the embedded web server application is developed and ported into Atmega8 with this setup. This single Atmega board has been act as data acquisition unit, control unit, embedded web server and self diagnosis. All processes are allocated with essential resources and associated with reliable scheduling algorithms and internet protocols followed by ARM processor. This

miniaturized setup reduces the complexity & size of system.

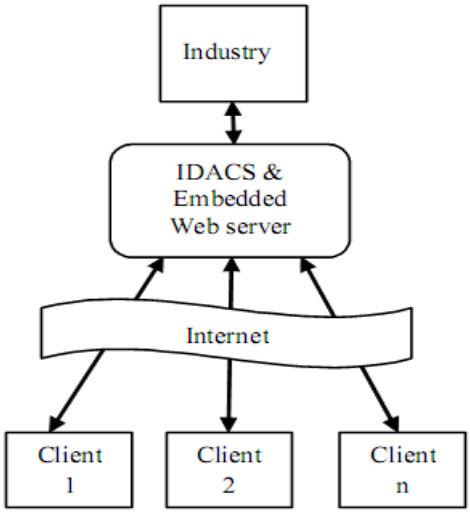


Figure 1. System overview

Fig.1 shows the overview of IDAC system. Every client can access the industry directly without any interaction with additional server and modules. IDACS shows Intelligent Data Acquisition and Control System. This system contains single Atmega8 processor which is portable with Real Time Linux RTOS. ARM processor is the heart of this work. It handles two modes at same time, DAC and Web server. During DAC mode Processor can measure signals which are coming from various external sources and applications. And it can control the industry machineries by the control instruction sent by client via embedded web server. During signal measurements Analog to digital converter is very important, because almost every external source is giving analog signal only. While converting these analog to digital processor has to handle asynchronous interrupts. This system uses RTLinux so it can handle many interrupts in an efficient manner because RTLinux has preemptive kernel with required privilege levels. Similarly during web server mode processor will handle client request and response to the particular client by sending web pages, client can interact the industry by giving instruction in web page on its own web browser. This setup can be suitable for inter communication with other nodes via Ethernet and higher end ports. Ethernet programming and execution is very easy and adaptable with various applications. Embedded web pages are designed by HTML language.

II. SYSTEM DESIGN

Hardware design, Software design and Porting are the entire important steps in whole system design.

A. Hardware design of the system

1) IDACS Design:

IDACS design is the major part in hardware. Atmega8 processor is a centre core of this system. The general hardware structure of the IDACS is shown in Fig 2. The online intelligent data acquisition and control system based on embedded Atmega platform has high universality, each acquisition and control device equipped with 24-way acquisition/control channels and isolated from each other. Each I/O channel can select a variety of electrical and non electrical signals like current, voltage, resistance etc., Digital acquisition are done by special ADC. The measured data are stored in external memory in which the memory is act as a data base during web server mode. The Atmega processor directly supports the Ethernet service and RS485 communication. Hence the data has been stored and controlled by some other PCs or network via RS485 & Ethernet. Atmega processor has internal I2C module. So it has the ability to communicate with any other peripherals.

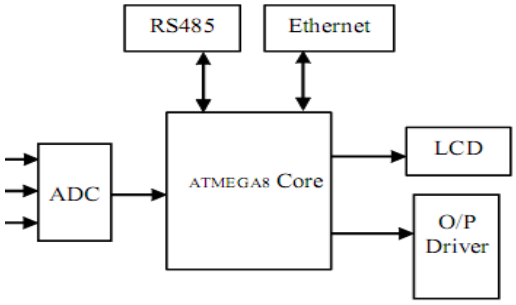


Figure 2. General Structure of the IDACS

I C is the wired communication protocol to communicate 2 with other processor or peripherals thro two wired link. This system has 128*64 LCD to display the information and measured parameters which makes the debugging and modification of the parameter easy. The Analog to digital interfacing module is independent with the embedded system, which is beneficial to the system maintenance and upgrade. As the embedded Ethernet interface makes the remote data exchange between the applications become very easy.

2) Analog to Digital Converter:

Fig 2. uses 16bit ADC chip AD7715. This is digital chip having I C module internally. It has the ability to transfer 2 the converted digital data to ARM processor. It needs only five lines, which are DOUT – Data output, DRDY – Data ready, DIN – Data Input, CS – Chip select and SCLK – system Clock. Converted digital data will be sending out by DOUT pin of the chip. This ADC chip is driven by

2.4576MHz crystal. It contains separate Reference signals Ref+ and Ref- and separate Analog input channels AIN+ and AIN- . During communication with ARM processor this ADC chip should be synchronized with the processor's clock.

3) RS485 Communication:

RS-485 is a telecommunications standard for binary serial communications between devices. It is the protocol orspecifications that need to be followed to allow devices that implement this standard to communicate with each other. This protocol is an updated version of the original serial protocol known as RS-232. While the original RS-232 standard allowed for the connection of two devices through a serial link, RS-485 allows for serial connections between more than 2 devices on a networked system.

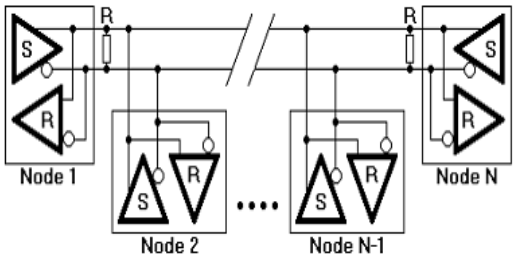


Figure 3. Network topology of RS485

The general network topology of RS485 is shown in Fig.3. Here N nodes are connected in a multipoint RS485 network. For higher speeds and longer lines, the termination resistances are necessary on both ends of the line to eliminate reflections. Use 100 Ω resistors on both ends. The RS485 network must be designed as one line with multiple drops, not as a star. RS-485 standard specifies up to 32 drivers and 32 receivers on a single (2-wire) bus. In this DACS system the RS485 communication is used to transfers the data between remote DACS to Embedded controller vice versa. New technology has since introduced "automatic" repeaters and high-impedance drivers and receivers such that the number of drivers and receivers can be extended to hundreds of nodes on a network. RS-485 drivers are now even able to withstand bus contention problems and bus fault conditions.A RS-485 network can be constructed as either a balanced 2 wire system or a 4 wire system. If a RS-485 network is constructed as a 2 wire system, then all of the nodes will have equal ranking. A RS-485 network constructed as a 4 wire system, has one node designated as the master and the remaining nodes are designated as slaves. Communication in such a system is only between master and slaves and never between slaves. This approach simplifies the software protocol that needs to be used at the cost of increasing the complexity of the wiring system slightly.

B. Software design of the system

1) Real Time Linux:

RTCore is a POSIX 1003.13 PE51 type real-time kernel, something that looks like a multithreaded POSIX process with its own internal scheduler. RTCore can run a secondary operating system as a thread, using a small virtual machine to keep the secondary system from disabling interrupts. This is a peculiar model: a UNIX process with a UNIX operating system as a thread, but it provides a useful avenue to modularity. RTLinux is RTCore with Linux as the secondary kernel. RTCore with BSD UNIX as the secondary kernel. Real-time applications run as real-time threads and signal handlers either within the address space of RTCore or within the address spaces of processes belonging to the secondary kernel. Real-time threads are scheduled by the RTCore scheduler without reference to the process scheduler in the secondary operating system. The secondary operating system is the idle thread for the real- time system. The virtual machine virtualizes the interrupt controller so the secondary kernel can preserve internal synchronization without interfering with real-time processing. Performance is adequate to allow standard PC and single board computers to replace DSPs in many applications.

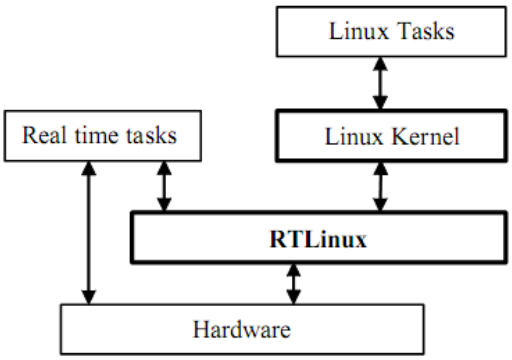


Figure 4. RTLinux Run time Model

Unlike Linux, RTLinux provides hard real-time capability. It has a hybrid kernel architecture with a small real-time kernel coexists with the Linux kernel running as the lowest priority task. This combination allows RTLinux to provide highly optimized, time-shared services in parallel with the real-time, predictable, and low-latency execution. Besides this unique feature, RTLinux is freely available to the public. As more development tools are geared towards RTLinux, it will become a dominant player in the embedded market. RTLinux is a typical dual-kernel, one is Linux kernel, which provides various features of general purpose OS, other one is RTLinux kernel, which support hard real time capability. Fig 4 illustrates the RTLinux architecture.

2) RTLinux Porting:

Real time modules (Declarations)

```
#include <rtl.h>
#include <time.h>
#include <rtl_sched.h>
pthread_t tasks[2];
void *idacs_thr(void *arg);
void *webserv_thr(void *arg);
RTLinux Modules (Init & Cleanup)
int init_module(void)
{
pthread_create(&tasks[0], NULL,
idacs_thr, NULL);
pthread_create(&tasks[1], NULL,
webserv_thr, NULL);
return 0;
}
void cleanup_module(void)
{
pthread_cancel(tasks[0]);
pthread_join(tasks[0], NULL);
pthread_cancel(tasks[1]);
pthread_join(tasks[1], NULL);
}
RTLinux Modules (RT Threads)
void *idacs_thr(void *arg)
{
pthread_make_periodic_np(
pthread_self(), gethrtime(),
5000000  00);
while(1)
{
pthread_wait_np();
rtl_printf("IDACS\n");
}
return 0;
}
```

3) Real Time Interrupts:
Hard Interrupts:
rtl request irq(3) and
rtl free irq(3)
these functions are used for installing and uninstalling hard
interrupt handlers for specific interrupts.

```
#include <rtl_core.h>
int rtl_request_irq(unsigned int irq,
unsigned int (*handler) (unsigned int,
struct pt_regs *));
int rtl_free_irq(unsigned int irq);
Soft Interrupts:
int rtl_get_soft_irq(
void (*handler)(int, void *, struct pt_regs *),
const char * devname);
void rtl_global_pend_irq(int ix);
void rtl_free_soft_irq(unsigned int irq);
```

The rtl get soft irq(3) function allocates a virtual irq number and installs the handler function for it. This virtual interrupt can later be triggered using rtl global pend irq(3). rtl global pend irq is safe to use from realtime threads and realtime interrupts. rtl free soft frees the allocated virtual interrupt.

4. TCP/IP in rtlinux:

LWIP is an implementation of the TCP/IP stack "Use of the LWIP stack is to reduce memory usage and code size, making LWIP suitable for use in small clients with very limited resources such as embedded systems". Improvements achieved by LWIP in terms of processing speed and memory usage have been performed by means of violating the TCP/IP layers. Most TCP/IP implementations keep a strict division between the application layer and the lower protocol layers. As the barrier between the kernel and the application processes is not a strict protection, a more relaxed scheme for communication between the application and the lower layer protocols can be performed by means of shared memory. In particular, the application layer can be made aware of the buffer handling mechanisms used by the lower layers. Therefore, the application more efficiently reuses buffers. Also, since the application process can use the same memory as the networking code the application can read and write directly to the internal buffers, thus saving the expense of performing a copy. As in many other TCP/IP implementations, the layered protocol design was used as a guide for the LWIP design and implementation. Each protocol is implemented as its own module, with a few functions acting as entry points into each protocol. Even though the protocols are implemented separately and as said before, some layer violations are made in order to improve performance both in terms of processing speed and memory usage. Hence many benefits can be obtained using RTL- LWIP. Besides providing lPV6 and TCP protocols, RTL- LWIP is more suitable for embedded systems, not only for its code but for its memory usage improvements.

III. RESULTS AND DISCUSSIONS

Fig 5 & 6 shows the few Simulation and execution results of ARM web server based DACS system using RTLinux.

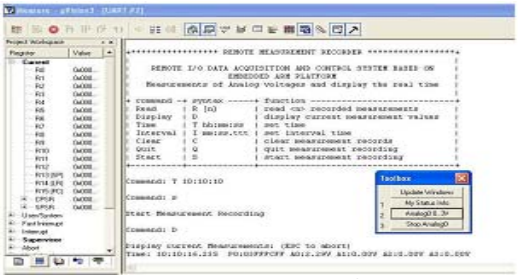


Figure 5. Simulation result of ADC

Figure 6. Kernel Configuration during NRT to RT Linux

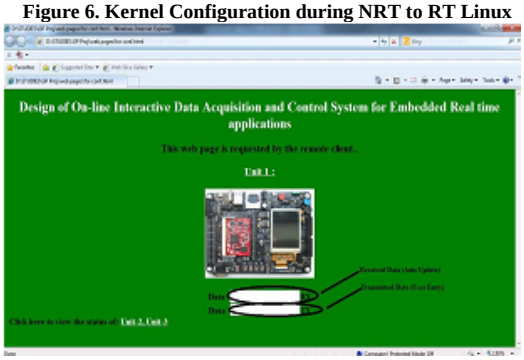


Figure 7. Web page requested by client

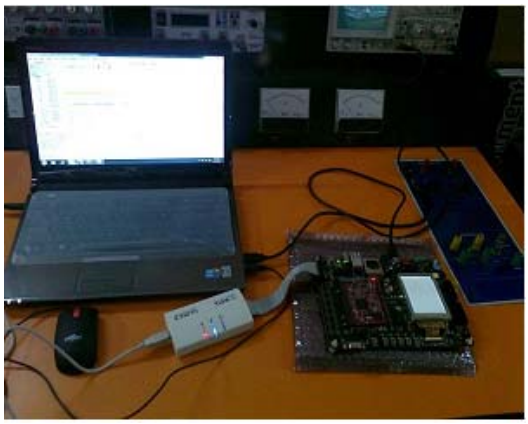


Figure 8. Host System and Hardware Target board

Figure 9. Web page sent by Target board to Client browser

Fig.7 is the simple web page designed using HTML language. It is requested by the client to server. Then the internet processes these request and server response for client request with web page. Now the Client can know the status of industry machineries and can control the machines via its own browser from remote location. It is showed in Fig.8&9. Hence, results show that the client can access the whole industry from any remote place via its own local browser. In industry the single Atmega8 board acts as data acquisition and control system and as web server, so the system is compact with less complexity. This system replaces the traditional system for remote access and control by embedded web server with Real Time Linux operating system. And this system is adaptable with kernel level debugging. It can be done by GDB, DDD Linux debuggers. These debuggers satisfy hard real time requirements by the use of RTLinux core.

IV. MERIT OF THE SYSTEM

A. Existing System

The use of single chip Data acquisition system (DAS) method in Instrumentation and process control application I not only limited in processing capacity and also the problem of poor real time and reliability. General web server require more resources and huge amount of memories. This system can only measure the remote signals and it cannot be used t control the process.

B. Proposed System

Limited processing capacity and the problem of poor real time and reliability of DAS system has been overcome by the substitution of embedded ARM processor for single chip method to realize interactive data acquisition and control (IDACS). This IDACS system can able to measure the remote signals and can control the remote devices through reliable protocols and communication network. Thi
system uses RTLinux Multi-tasking operating system to measure and control the whole process. And the embedded web server mode requires less resource usage, high reliability, security, controllability and portability.

V. CONCLUSIONS

With the rapid development of the field of industrial process control and the wide range of applications of network, intelligence, digital distributed control System, it is necessary to make a higher demand of the data accuracy and reliability of the control system. This embedded ARM system can adapt to the strict requirements of the data acquisition and control system such as the function, reliability, cost, size, power consumption, and remote access and so on. This system operated by DACS mode to acquire the signals and control the devices remotely. Embedded web server mode is used to share the data

with clients in online. Both modes are efficiently carried out by real time multi tasking operating system (RTLinux). This system can be widely applied to electric power, petroleum, chemical, metallurgy, steel, transportation, Electronic & Electrical industries, Automobiles and so on.

REFERENCES

[1]. S.Li,Jiarong, R.Luo, YichunC.Wu, GuimingM.Li, FengWang, and YongWang. "Continuous and Real-Time Data Acquisition Embedded System for EAST", IEEE Trans. Nuclear science,Vol.57,No.2, pp. 696-699, April 2010

[2]. K.JackerandJ.Mckinney,"TkDAS- A data acquisition system using RTLinux, COMEDI, and Tcl/Tk," inProc. Third Real Time Linux Workshop, 2001. [Online].Available: The Real Time Linux http://www.realtimelinuxfoundation.org/events/rtlws-2001/papers.html

[3]. E.Siever, A.Weber, S.Figgins, and R.Love, CA:O'Reilly, "Linux in a Nutshell,",2005.

[4]. Clyde C. W. Robson, Samuel Silverstein, and Christian Bohm ,"An Operation-Server Based Data Acquisition System Architecture," IEEE Trans. Nuclear science, Vol. 55, No. 1, February 2008.

[5]. J. E. Marca, C. R. Rindt, M. Mcnally, and S. T. Doherty, "A GPS enhanced in-vehicle extensible data collection unit," Inst. Transp. Studies, Univ. California, Irvine, CA, Uci-Its-As-Wp-00-9, 2000.

[6]. Y. C.Wu, J. R. Luo, and J. Z. Shan, "Development of the central timing system on the EAST Tokamak," IEEE Trans. Nuclear science, Vol. 30, No. 9, pp. 789Á2, 2007.

[7]. F. Acernese, P. Amico, M. Alshourbagy, F. Antonucci, S. Aoudia, P. Astone, S. Avino, D. Babusci, G. Ballardin,"Data Acquisition System of the Virgo Gravitational Waves Interferometric Detector,"IEEE rans. Nuclear science , Vol. 55, No. 1, pp.225-232, February 2008

SIMULATION OF POWER QUALITY IMPROVEMENT USING SHUNT ACTIVE POWER FILTER USING SPACE VECTOR PULSE WIDTH MODULATION TECHNIQUE (SVPWM)

MOHD AFROSE AHMED & P.NAGESWARA RAO

Abstract :- This project presents a control method for shunt active power filter using Space Vector Pulse Width Modulation (SVPWM). In the proposed control method, the Active Power Filter (APF) reference voltage vector is generated instead of the reference current, and the desired APF output voltage is generated by SVPWM. A MATLAB code is developed to generate the SVPWM switching pulses fed to the two-level inverter topology. The entire power system block set model of the proposed scheme has been developed in MATLAB environment. The developed control algorithm is simple. The APF based on the proposed method can eliminate harmonics, compensate reactive power and balance load asymmetry. Simulation results show the feasibility of the APF with the proposed control method.

INTRODUCTION

GENERAL

The growing use of non-linear and time-varying loads has led to distortion of voltage and current waveforms and increased reactive power demand in ac mains. Harmonic distortion is known to be source of several problems, such as increased power losses, excessive heating in rotating machinery, and harmonic resonances in the utility, significant interference with communication circuits, flicker and audible noise, incorrect operation of sensitive loads [1, 2].

Traditionally, LC tuned passive filters have been used to absorb harmonic currents generated by nonlinear loads. Their main advantage is high reliability and low cost. However, passive filters have several drawbacks, which may cause harmonic interaction with the utility problems with the utility system, in the presence of stiff utility sharp

tuning of the LC filter is required and may not meet the specified harmonic current limits [3, 4]. This provides the motivation for investigation of an active filter topology, which is practically viable, cost effective and can meet the recommended standard for high power nonlinear loads. For high-power applications, the active filters are not cost effective due to their large rating and high switching-frequency requirement of the Pulse Width Modulation (PWM) inverter.

ACTIVE POWER FILTERS

INTRODUCTION

In a modern power system, the growing use of non-linear loads and time-varying loads are increasing. These nonlinear loads may cause poor power factor, high degree of harmonics and distortion of current and voltage waveforms. These problems are solved by using APF's. By implementing these for power conditioning, it provides functions such as reactive power compensations, harmonic compensations, negative-sequence current or voltage compensation and voltage regulation. The main purpose of the APF installation by individual consumers is to compensate current harmonics or current imbalance of their own harmonic-producing loads. Besides that, the purpose of the APF installation by the utilities is to compensate for voltage imbalance or provide harmonic damping factor to the power distribution systems. Fig.2.1 shows the basic APF block diagram including non-linear load on three-phase supply conditions.

APF consisting of VSI and a dc capacitor have been researched and developed for improving the power factor and stability of transmission systems. APF have the ability to adjust the amplitude of the synthesized ac voltage or current of the inverter by means of pulse width modulation or by control of dc-link voltage, thus by drawing either leading or lagging reactive power from the supply. APF is an up-to-date solution to power quality problems. Normally, APF can be classified into shunt and series. Both are designed to compensate for reactive power or harmonics. APF consists of an inverter with switching control circuit. The inverter of the APF will generate the desired compensating harmonics based on the switching gates provided by the controller. The APF injects an equal-but-opposite distortion harmonics back into the power line and cancel with the original distorted harmonics on the line. Fig.2.1 shows the basic idea for the compensation principle of an APF.

The line current, i_s is shaped to be sinusoidal by adding the compensating current, i_f into the distorted load current, i_l. The problem of this APF is the suitable design for the controller and the filter configuration. Traditionally, its control techniques were mostly using Pulse Width Modulation (PWM) technique. However, before developing the controller, the configuration of the APF used in the design has to be defined.

CLASSIFICATION OF APF

APF's are divided into dc and ac filters. The dc filters are designed to compensate for current or voltage harmonics on the dc side of thyristor converters for HVDC systems and the dc link rectifier or inverter for traction systems. The ac filters are normally designed for the ac power system harmonic compensations. However, the APF is usually referred to the active ac power systems. There are various types of APF's and these can be classified into different categories based on the system configuration, the power circuit, the control strategy and techniques.

Classification by system topology

The topologies of the active filters are the shunt, series and hybrid active passive power filter. The shunt APF is controlled to draw and inject compensating current, i_f to the power system and cancel the harmonic currents on the ac side of a general purpose rectifier**.** Besides that, it has the capability of damping harmonic resonance between an existing passive filter and the supply impedance.

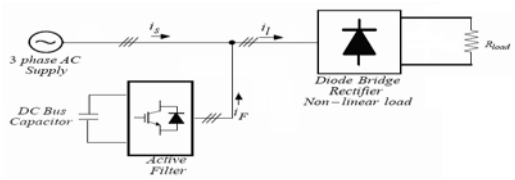


Fig.1 Shunt APF

The series APF is connected in series with the utility by a matching transformer. Normally, this filter is suitable for harmonic compensation of a voltage harmonic source such as diode rectifier with a dc link capacitor. The difference of the shunt and series active filter is the compensating harmonic injection method and the type of compensating harmonic.

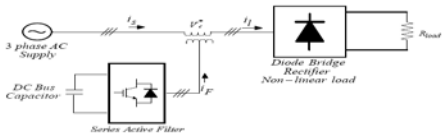


Fig.2 Series APF

The difference of the shunt and series active filter is the compensating harmonic injection method and the type of compensating harmonic. The shunt and series active filters act as a current source with i_f and a voltage source with V_C* respectively in order to compensate the harmonics currents or voltages occurred in the distorted line. Shunt APF also compensates reactive power and the series active power filters can be used for ac voltage regulation.

Another type of active filter configuration is the Hybrid Active-Passive Filters (HAPF). The HAPF's consists of the combination of the active and passive filters. The series active filter with shunt passive filter is usually used in testing field. In this project, the HAPF is formed by a single tuned LC filter per phase and a three phase active filter, which are directly connected in series without any matching transformer. Thus, no additional switching-ripple filter is required for the active filter because the LC filter functions not only as a harmonic filter but also as a switching-ripple filter.

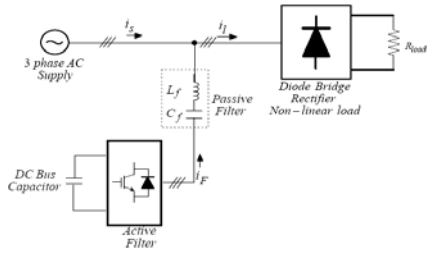


Fig 3 High Pass Active Filter

SPACE VECTOR PULSE WIDTH MODULATION FOR THE TWO- LEVEL INVERTER TOPOLOGY

THEORY OF SVPWM TECHNIQUE

SVPWM technique was originally developed as a vector approach to pulse–width modulation for three-phase inverters. The SVPWM method is frequently used in vector controlled applications. In vector controlled applications this technique is used for reference voltage generation when current control is exercised. It is a more sophisticated, advanced, computation intensive technique for generating sine wave that provides a higher voltage with lower total harmonic distortion and is possibly the best among all the pulse width modulation techniques. It confines space vectors to be applied according to the region where the output voltage vector is located. Because of its superior performance characteristics, it is been finding wide spread applications in recent years. The main aim of any modulation technique is to obtain variable output voltage having a maximum fundamental component with minimum harmonics. Many PWM techniques have been developed for letting the inverters to posses various desired output characteristics to achieve the wide linear modulation range, less switching losses, lower harmonic distortion. The SVPWM technique is more popular than conventional technique because of its excellent features. (1). More efficient use of DC supply voltage. (2). 15% more output voltage then conventional modulation. (3). Lower total Harmonic distortion. (4). Prevent un-necessary switching hence less commutation losses.

3.3 PRINCIPLE OF SVPWM

Firstly model of a three-phase inverter is presented on the basis of space vector representation. The three-phase VSI is reproduced in Fig.3.1. $S_1$to S_6 are the six power switches that shape the output, which are controlled by the switching variables a, a', b, b', c and c'. When an upper transistor is switched on, i.e., the corresponding a', b', or c' is 0. Therefore, the on and off states of the upper switches S_1, S_3, S_5 can be used to determine the output voltage. The relationship between the switching variable vector [a, b, c]^t and line-to-line voltage vector [V_{ab} V_{bc} V_{ca}] is given by (3.1) in the following**:**

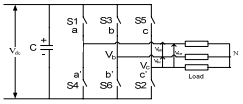


Fig 4 Power circuit of a three-phase VSI

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = V_{dc} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (3.1)$$

Also, the relationship between the switching variable vector [a, b, c]^t and the phase voltage vector [V_a V_b V_c]^t can be expressed below.

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{V_{dc}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (3.2)$$

There are eight possible combinations of on and off patterns for the three upper power switches. The on and off states of the lower power devices are opposite to the upper one and so are easily determined once the states of the upper power transistor are determined.

PROPOSED CONTROL METHOD USING SVPWM

BLOCK DIAGRAM OF CONTROL SYSTEM

The main section of the APF shown in Fig. 5 is a forced-commutated VSI connected to dc capacitor.

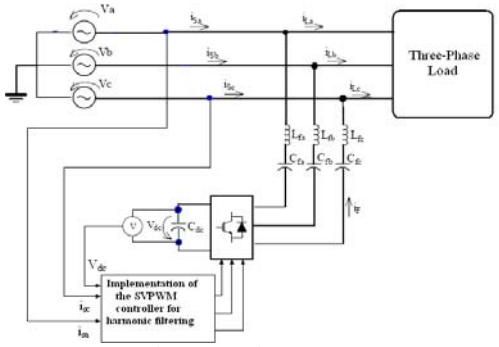


Fig.5 Configuration of an APF using SVPWM

Considering that the distortion of the voltage in public power network is usually very low, it can be assumed that the supply voltage is ideal sinusoidal and three-phase balanced as shown below:

$$\left.\begin{aligned} v_{sa} &= V_s \sin(\omega t) \\ v_{sb} &= V_s \sin(\omega t - 2\pi/3) \\ v_{sc} &= V_s \sin(\omega t + 2\pi/3) \end{aligned}\right\} \quad (4.1)$$

where $\overline{V}_s$ is the supply voltage amplitude

It is known that the three-phase voltages [v_{sa} v_{sb} v_{sc}] in a-b-c can be expressed as two-phase representation in d-q frame by Clark's transformation and it is given by

$$\overline{V}_s = \begin{bmatrix} V_d \\ V_q \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} \quad (4.2)$$

It is possible to write equation (4.2) more compactly as

$$\overline{V}_s = \frac{2}{3}\left(v_{sa}a^0 + v_{sb}a^1 + v_{sc}a^2\right) = V_{sd} + jV_{sq} = V_s \angle \theta^s$$

where $a = e^{j\frac{2}{3}\pi}$, so balanced three-phase set of voltages is represented in the stationary reference frame by a space vector of constant magnitude, equal to the amplitude of the voltages, and rotating with angular speed $\omega = 2\pi f$.

As shown in Fig.5, the shunt APF takes a three-phase voltage source inverter as the main circuit and uses capacitor as the energy storage element on the dc side to maintain the dc bus voltage V_{dc} constant. Fig.6 shows the per-phase (Phase A) equivalent circuit of the system described in Fig.4.1.

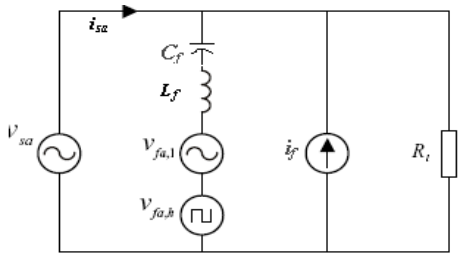
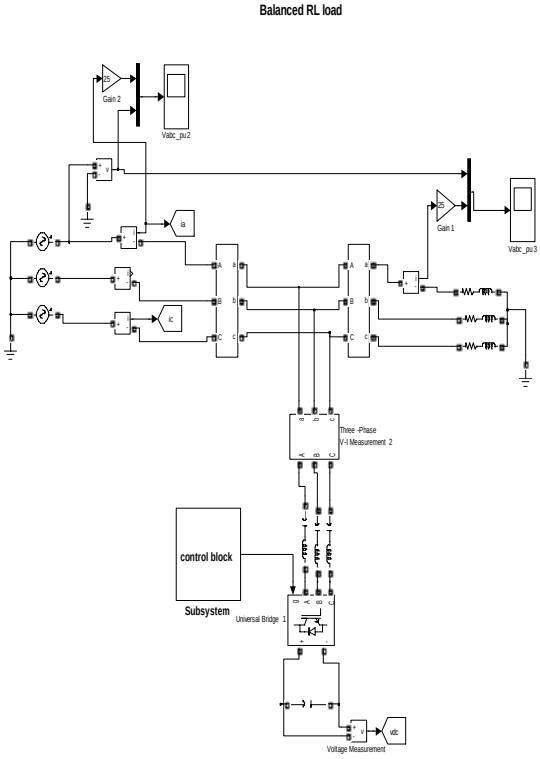


Fig.6 Equivalent circuit of a simple power system together with the APF

SIMULATION RESULTS

The developed control method for three-phase shunt APF is simulated in MATLAB/Simulink. Firstly, the three-phase supply currents are sensed and transformed into synchronous reference frame (d-q) axis. The fundamental component of the supply current is transformed into dc quantities in the (d-q) axis and the supply current amplitude I_s generated by the PI controller. The obtained d-q axis components generate voltage command signal. By using Fourier magnitude block, voltage magnitude and angle is calculated from the obtained signal. These values are fed to the developed code and generated switching actions are applied to the APF. Thus, power balancing of the filter takes place. Further, the performance with different type of loads is presented.



For balanced RL load

Source current and load current are scaled by factor 25 for comparison purpose.

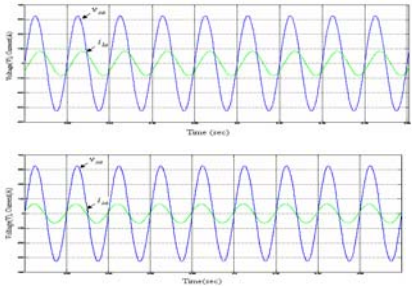


Fig.7 Simulation results of balanced linear load

(a) The phase-A supply voltage and load current waveforms
(b) The phase-A supply voltage and supply current waveforms

The Fig.7 shows the simulation results of the APF when load is three-phase balanced RL load. Fig.7 (a) is the waveforms of the phase-A supply voltage and the load current before compensation. Fig.7 (b) is the waveforms of the phase-A supply voltage and the supply current after compensation.

For Unbalanced RL load

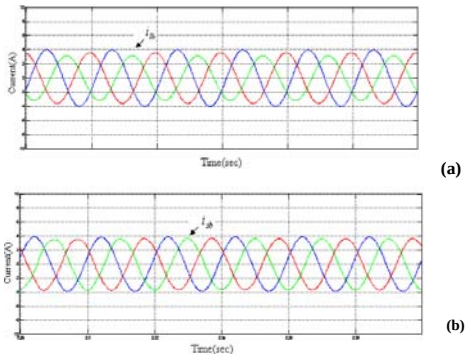


Fig.8

Simulation results of unbalanced RL Load
(a) Three-phase load current waveforms
(b) Three-phase supply current waveforms

The Fig.8 shows the simulation results of APF when three-phase unbalanced RL load is considered. Fig.8 (a) is the waveforms of the three-phase load current before compensation. Fig.8 (b) is the waveforms of the three-phase mains current after compensation. From the figures, it can be seen that APF controller can remedy the system unbalance.

5.2.3 For Non-Linear Load with Resistance

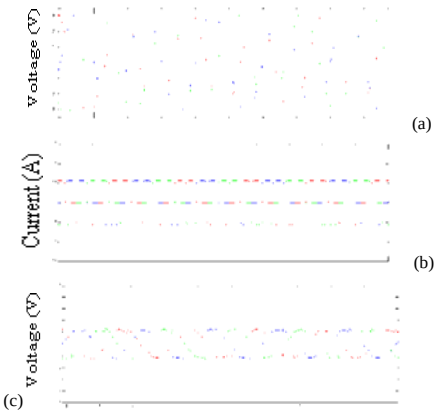


Fig.9 Simulation results of non-linear load

(a)The three-phase source voltage waveforms
(b) The three-phase load current waveforms
(c) The three-phase source current waveforms

The Fig.9 shows the behavior of the APF when the non-linear load is a three-phase diode bridge rectifier with resistance load. Fig.9 (a) is the waveforms of the source phase voltage. Fig.9 (b) is the wave forms of the load current before compensation. Fig.9 (c) is the waveforms of the supply current after compensation.

(a) (b)

Fig 10 Harmonic spsectrum of non linear loads
(a) Phase A load current harmonics spectrum
(b) Phase A load current harmonics spectrum

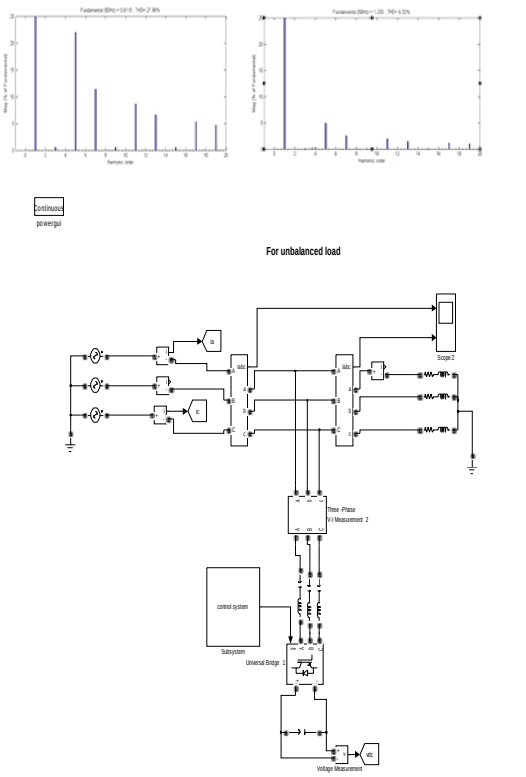


Fig.11 Simulation model of APF with non-linear load

CONCLUSION

In this project, a control methodology for the APF using SVPWM is proposed. This method requires few sensors, simple in algorithm and able to compensate harmonics and unbalanced loads. The performance of APF with this method is done in MATLAB/Simulink. The algorithm will be able to reduce the complexity of the control circuitry. The harmonic spectrum under non-linear load conditions shows that reduction of harmonics is better.

Under unbalanced linear load, the magnitude of three-phase source currents are made equal and also with balanced linear load the voltage and current are made in phase with each other. The simulation study of two level inverter is carried out using SVPWM because of its better utilization of dc bus voltage more efficiently and generates less harmonic distortion in three-phase voltage source inverter. This SVPWM control methodology can be used with series APF to compensate power quality distortions.\

REFERENCES:

[1] EI-Habrouk. M, Darwish. M. K, Mehta. P, “Active power filters-A review,” Proc.

IEE-Elec. Power Applicat., vol. 147, no. 5, Sept. 2000, pp. 403-413.

[2] Akagi, H., “New trends in active filters for power conditioning,” IEEE Trans. on Industry applications, vol. 32, No. 6, Nov-Dec, 1996, pp. 1312-1322.

[3] Singh.B, Al-Haddad.K, Chandra.A, “Review of active filters for power quality improvement,” IEEE Trans. Ind. Electron., vol. 46, No. 5, Oct, 1999, pp. 960-971.

[4] Ozdemir.E, Murat Kale, Sule Ozdemir, "Active power filters for power compensation under non-ideal mains voltages," IEEE Trans. on Industry applications, vol.12, 20-24 Aug, 2003, pp.112-118.

[5] Dan.S.G, Benjamin.D.D, Magureanu.R, Asimionoaei.L, Teodorescu.R, Blaabjerg.F, "Control strategies of active filters in the context of power conditioning," IEEE Trans. on Ind. applications,vol.25,11-14 Sept-2005, pp.10-20

[6] Wang Jianze, Peng Fenghua, Wu Quitao, Ji Yanchao, "A novel control method for shunt active power filters using svpwm," IEEE Trans. on Industry applications, vol.1, 3-7 Oct, 2004, pp.134-139.

[7] Atif Iqbal, Lamine.A, Imtiaz.Ashraf, Mohibullah, "Matlab model of space vector pwm for three-phase voltage source inverter," universities power engineering conference, 2006, UPEC'06, proceedings of the 41st international volume 3, 6-8 Sept. 2006, pages:1096-1100.

[8] Rathnakumar.D, LakshmanaPerumal, Srinivasan.T, "A new software implementation of space vector pwm," IEEE Trans. Power Electron., vol.14,8-10 April 2005, pp.131-136.

Mohd Afrose Ahmed is the M.Tech student with specialization of Power Electronics, in the department of electrical and electronics engineering at Lords Institute of Engineering and Technology, Hyderabad, A.P, India and B.Tech from JNTU Hyderabad, India.

P.Nageswara Rao is an associate professor in Electrical and electronics engineering department at Lords Institute of Engineering and Technology, Hyderabad, A.P, India. Research areas of interests are fuzzy logic applications in power systems, Applications of FACTS controllers in Power Systems. B.Tech from JNTU, Hyderabad, India and M.Tech (Power systems) from Acharya Nagarjuna University, India.

◈◈◈

THE SAPPER – A GAME IMPLEMENTED USING OPENGL

KRISHNA BHARGAVA M L, K S SHRIVARA AND ANITHA PREMKUMAR

Department of Computer Science and Engineering, Sir M Visvesvaraya Institute of Technology

Abstract –This paper is focused on an intuitive way to create a simple game in OpenGL, which is both user involving, as well as demonstrative of the power of OpenGL in computer graphics. The game named "The Sapper", assigns to the user, the role of a sapper, who is a soldier performing several military engineering duties, of which laying and clearing minefields is one. The game simulates this environment, where the player has to move through an enemy guarded area, and diffuse bombs, remaining undetected throughout the mission. The visible game components are developed as OpenGL graphics, implemented in an intuitive way, having textured tiles, character sprites and other graphical elements. This is combined with gameplay elements that results in a simple game that runs efficiently on most computer systems. The success of this implementation approach on a small scale opens a possibility for it to be used in developing larger, more complex games.

I. INTRODUCTION

In today's digital revolution, computer graphics plays a vital role in a myriad of areas encompassing the animation, movie and video game industry. Computer games are one of the oldest forms of video games, with a user base of millions of people, not having an age group as a barrier. This paper on creating a game uses the Open Graphics Library (OpenGL) to create a realistic graphics environment, around which a simple gameplay is built. OpenGL is a widely used standard specification defining cross-language, multi-platform, 2D and 3D graphics application programming interface (API). The environment in this game is 2 dimensional, which is made up with the use of textured images and other graphic components representing the playing area, the player and other characters and miscellaneous elements.

II. FUNDAMENTALS

The game is developed using the C++ programming language on the Microsoft Visual Studio Interactive Development Environment, specifically the Visual C++ environment. The graphics involved in the game are developed using the OpenGL Graphics Utility Toolkit (GLUT) API. The game can be run on the Microsoft Windows Operating System, as it is deployed in the form of an executable application (.exe) along with supporting data files. The API definitions file "glut.h", the library file "glut32.lib" and the "glut32.dll" system linking and deploying the source code of the game. The above files are to be placed in the absolute paths in Windows as given in Table 1.

TABLE I [1]

glut.h	C:\Program Files\Microsoft Visual Studio\VC\include\GL
glut32.lib	C:\Program Files\Microsoft Visual Studio\VC\lib
glut32.dll	C:\Windows\System

III.IMPLEMENTATION

A straight-forward approach to creating a game has been used, where the graphics and gameplay are developed as separate modules, and eventually brought together to obtain the desired result.

A. Graphics

The entire graphics has been implemented using Open Graphics Library (OpenGL). It is a widely used standard specification that defines functions as a part of an Application Programming Interface(API) to describe 2D and 3D environments. Specifically, the OpenGL Utility Toolkit (GLUT), which is a portable API well suited for small to medium sized graphics applications is used. GLUT provides the essential communication link to the windowing system [3]. However, it also includes definitions of all API functions that are a part of the GL and GLU libraries. GL and GLU provide graphics drawing capabilities. Thus, GLUT is sufficient to develop all graphics aspects of the game.

A Map is the area visible to the user while playing each level of the game. It is the most graphics intensive part of the game implementation. The size of the map in terms of pixels is defined by the resolution of the display device on which the game is being played on. The entire map area is made up of a collection of square shaped, same sized tiles. The top-most row of tiles is assigned to display various gameplay information, while the rest of them are used for the actual gameplay. The other graphics components drawn on the map include: sprites representing the player and enemy soldiers, bombs to be diffused and some text elements.

Graphics is also used in other parts of the game including various splash screens and the main menu. The various graphics components are described in the following sections:

1) Tiles

Tiles are the smallest units of a map. The game uses tiles of 32x32 pixels in size. Thus, the number of tiles in a map is dependent on the resolution of the map. Different types of tiles when put together in an orderly manner create the playable area of the map. Each type of tile used make up the floor and various wall orientations, with a different texture making up each of these tile types.

2) Textures and Sprites

Textures allow us to glue an image to a polygon and to draw the image as a single polygon. Texture mapping allows us to easily transform and render the images [4].Textures and character sprites are created using images created using image manipulation software. Images are sized as 32x32 pixels each, in order to correspond to the size of the tiles. Thus, each character spirit can cover an area of one tile size. Textures are imported from the secondary storage and stored in the primary memory before the map representing a level is loaded. The textures are then redrawn at regular intervals corresponding to the movement of the sprites.

3) Animation

The character sprites are animated using a simple but, intuitive technique. Up to nine images are used for a single character sprite. Each of these images are associated with a specific direction that the character can move in. As the sprite moves on the map, the change in direction if any is observed and corresponding image with respect to the new direction is loaded and the screen redrawn. Each direction is also associated with multiple images, and changing these images for each movement in the same direction as well as movements in other directions creates an apparent effect of animation.

4) Text and miscellaneous

Text is drawn on to the screen using outline fonts. Outline fonts offer flexibility as they can be in 2D or 3D, and basic OpenGL transformations of translation, rotation and scaling to be used on them to manipulate their size, position and orientation on the screen [2]. Text is used to display game information, to make up the main menu and to offer interactive information to the user.

B. Data Handling

Levels in the game are represented using maps. Each map which consists of tiles are stored as a separate file entity. Each tile is represented by a single byte in the file. A pre-defined number is assigned to each type of tile. Before each map is loaded, this file is read. For example, if the number stored in the file is 1 and 1 is associated with the floor tile type, then a floor type tile is understood to be placed in that position on the map. Thus, the information stored in the map file represents the tiles placed in order and subsequently define the playable area of the map.

A separate file is maintained to record information about the initial position of the player, the bomb and the desired movements of the enemy soldiers. The above two files when combined provide complete information that is necessary to display all the components of the map.

These two files are generated using a separate map creation utility which allows easier and faster creation of a map. The utility allows the map creator to place tiles as desired, so as to form a desired playing area. For example, two rows of tiles can be placed with the rows in between them filled with floor tiles. After the playing area is created, the initial position of the player is marked, followed by the position of the bomb. The last task is to provide the initial position of the various enemy soldiers along with the pre-defined paths in which they would move. After all this has been taken care of, the entire data collected is written onto the corresponding files. The generated files are now ready to be read by the game.

Images which are used to represent the tiles and character sprites are stored in the RAW image format. The RAW format allows images to be imported faster even though they occupy a considerable amount of space when compared to other traditional formats [5]. These images are imported in the game and stored as textures which can then be used to draw the map after referencing the information from the map files and the character sprite files.

C. Gameplay

The game revolves around the concept of a sapper diffusing a live bomb in a given area that is defined by a map. The sapper has to achieve this task without getting caught by the enemy soldiers. A certain amount of time is required to diffuse the bomb in each level. This is indicated by a progress bar, which fills up as the bomb is being diffused. The following sections describe the various concepts that have been used in order to achieve this gameplay implementation:

1) Field of view

The area of the map that is visible at any given time for the player and enemy soldiers is limited by their respective fields of view (FOV). The FOV of the player is limited to a 9x9 square tile units with the player in the center. Similarly, each enemy soldier's

FOV is limited to a 3x3 square tile units. As the player and enemy soldiers move, their FOVs are updated accordingly. Since the FOVs of the player and enemy soldiers vary an enemy soldier maybe visible to the player but not vice-versa.

2) Collision Detection

Collision detection is the principle concept behind the gameplay. It has been used for two purposes as described below:

- *Character Movement Restriction*

A player can move around the map only on the floor tiles. The primary goal is to ensure that the player does not pass through walls bounding the play area. This is done by using the current tile on which the player is, and comparing it with the tile the player would move to, with respect to the direction indicated by the key pressed. The player's tile position is updated only if his next position is on a floor tile. If the next position corresponds to a wall tile, then the player's position is not changed.

- *Character – Character Interaction*

Collision detection determines the act of the player getting caught by the enemy soldiers. FOV is used in order to implement this technique. The player's current position in terms of the tile on which he is standing on is compared with the FOV of each of the enemy soldiers. In case the player's tile overlaps with even one tile in the FOV of any of the enemy soldiers, it means that the particular enemy soldier has the player in sight and can shoot him down. This leads to the player's death and the game ends. Thus, each level continues until the player gets caught, or he succeeds in diffusing the bomb on that level, in which case, the next level is loaded.

3) Difficulty

Each level has a different map. With subsequent levels of the game, the map complexity is increased. This is done by creating a larger playable area, having more number of guards, and making the guarding heavier near the location of the bomb. Ultimately, with each passing level, the task for the player becomes more challenging due to increasing difficulty levels.

4) Interaction with user

The designer's task is to keep the user interface rules and vocabulary simple and to use the concepts that the user already knows or can learn easily [6]. The user being the player of the game interacts completely through the keyboard. The W, S, A, D keys are used for player movement in – game, as well as to navigate through the main menu and other screens. The Q key is used to exit the current screen.

The Spacebar is used in – game to diffuse the bomb. The player has to navigate to the location of the bomb, and press and hold the Spacebar. On doing this, the progress bar on the top of the screen starts to fill up, and the bomb gets diffused on its complete filling. Releasing the space bar when the bomb is being diffused, allows the player to move out of the bomb location in case he senses an enemy soldier closing in. The progress bar remains at the same state, and the player can come back after the area is clear of enemy soldiers and continue diffusing the bomb from the state where he had left off.

IV. SCREENSHOTS

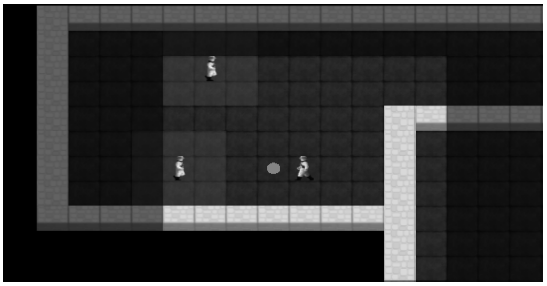


Fig. 1

Figure 1 shows a region of the map with the Field of Views of the player and two enemy soldiers. It can be seen that the player's FOV is much larger compared to the soldiers' FOVs. The location of the bomb is shown with the player approaching to diffuse it. Also, the other features of the map such as the floor and wall tiles are visible.

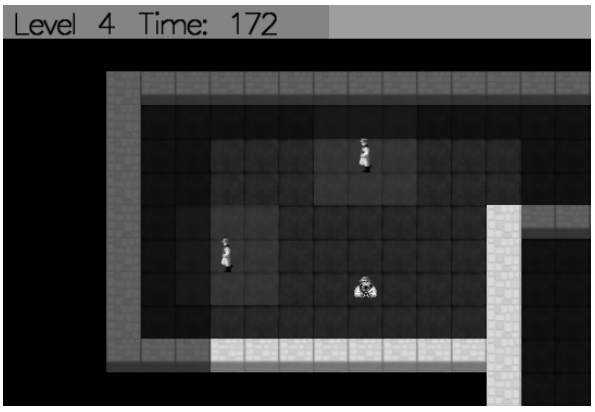


Fig. 2

Figure 2 shows the bomb being diffused. The level information along with the progress bar is shown on the top. The bar fills up as the bomb gets diffused. The time elapsed since the level started is also shown.

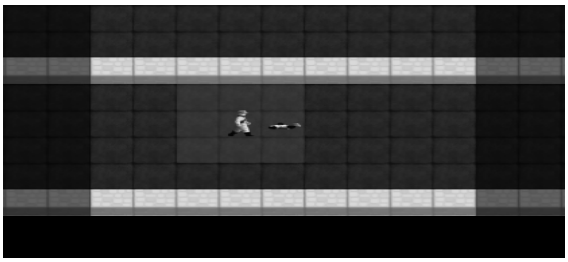


Fig. 3

In Figure 3 the soldier's Field of View overlaps with the player's current position which results in the death of the sapper. This ends the game.

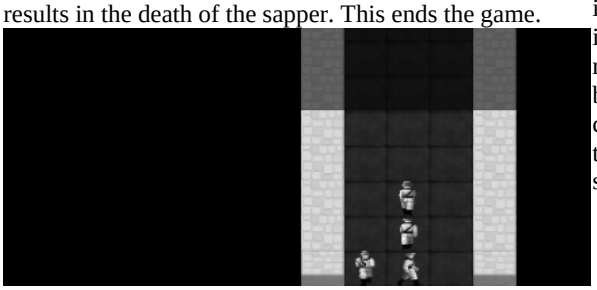


Fig. 4

Figure 4 shows an overlap of four images depicting consecutive positions of the player. This is shown in order to demonstrate how animation is done in the game.

V. RESULTS

The result of running the game on many computers, each having a different configuration was measured in terms of frames per second. The results of four configurations are summarized in the graph shown in Figure 5.

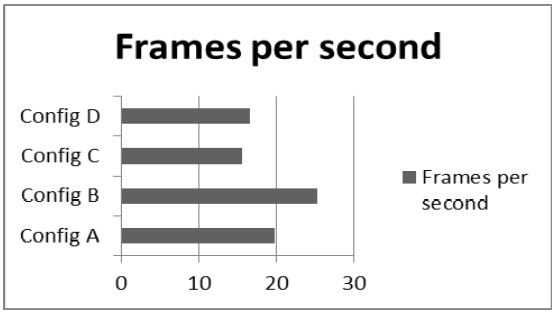


Fig. 5

Configurations tested:

Config A: Intel Core i5 2430M, 4GB RAM, NVidia GT540M

Config B: Intel Core i5 750, 4GB RAM, NVidia GTX260

Config C: AMD Athlon x64, 2GB RAM, Intel HD2500

Config D: AMD Phenom X4 940, 2GB RAM, AMD Radeon 3300

It is observed that the game performs efficiently in the computers tested above. The dip in frame rates is observed with slightly older configurations.

VI. FUTURE ENHANCEMENTS

Even though the game is sufficiently complete in demonstration of the power of OpenGL, there are some areas where improvements are possible. Code optimization may provide a little increase in the frame rates. Also, there is scope for implementing a scoring system, and maintaining records of previous scores such that high scores can be calculated and displayed in order to provide a competitive game. Audio can be added to improve the overall experience of the game. There is also scope for improvement in graphics.

VII. CONCLUSION

The game serves as an important learning tool for people who are just touching the surface of the deep ocean, which is OpenGL. Also, the game demonstrates how OpenGL can be used to create games that look sophisticated, yet are easy in their implementation and simple and clean in their design. From the user's perspective, the game provides enough challenges by increasing the difficulty in subsequent levels, and also keeps the player involved through both the gameplay as well as the graphics. The success of this game on a small scale opens up a wide avenue for using this model in creation of larger, more complex games.

REFERENCES

[1] Edward Angel – Interactive Computer Graphics: A Top-Down Approach Using OpenGL, Pearson/Addison-Wesley, 2009.

[2] Outline Fonts tutorial – NeHe productions available at http://nehe.gamedev.net/tutorial/outline_fonts/15004/

[3] GLUT – The OpenGL Utility Toolkit referred from: http://www.opengl.org/resources/libraries/glut/

[4] Mason Woo (Author), Jackie Neider (Author), Tom Davis (Author), OpenGL Architecture Review Board (Corporate Author) – OpenGL Programming Guide: The Official Guide to Learning OpenGL, Version 1.1 (Otl), Addison-Wesley Pub (Sd); 2nd edition (January 1997).

[5] Ron Fosner - "OpenGL Programming for Windows 95 and Windows NT", Addison-Wesley Developer's Press, 1997.

[6] James D Foley, Andries van Dam, Steven K. Fenier and John F. Hughes - "Computer Graphics, Principle and Practice", Addison-Wesley Professional, 1995, 2nd Edition.

◈◈◈

DRASTIC CHANGES IN MEDICAL FIELD BY THE INVENTION OF NANOBOTS

L.JAGJEEVANRAO, R.PRASANNA, A.SOWJANYA & K.MANASASAISITA

School of Computing, KLUniversity, GunturDt, India

Abstract-Nanorobot (nanobots, nanoids, nanites) is a small electromechanical device with an exterior made up of carbon atoms in a diamond shape is used to interact with nanoscale objects or manipulate with nanoscale resolution. Usually the size of these robots range from 500-3000nm. In surgery this is more accurate instead of using the human hand. Nanobots moves around their environment consuming molecules to attain energy. Nanobots direct themselves towards certain cells by their glycolipid structures. This idea would help physicians to treat diseases effectively without any adverse side-effects, actually the idea is to repair organs such as the brain, or the heart. The most valuable feature is that without any invasive surgery all of this can be done.

Keywords*- nanoscale, glycolipid, invasive,nanobots*

INTRODUCTION

- *What is Nanobot?*

Nanorobots are minute robots, similar to the size of molecules, and are used in the improvement of innovative treatments in medicine and other biological applications[3]. There are even possible applications in which nanorobots could be used to help, mend or repair damaged tissue within a person's body. Nanobots will find their first applications in medical science also known as nanomedibots.

- *Structure:*

They will have a diameter of about 0.5 to 3 microns and will be constructed out of parts with dimensions in the range of 1 to 100 nanometers. The main element used will be carbon in the form of diamond / fullerene nanocomposites because of the strength and chemical

inertness of these forms.Nanorobots, measure only about six atoms wide[8], so they are capable of building with the very particles of our bodies: atoms and molecules. It is anticipated that they could be equipped with all sorts of tools and cameras in order to furnish more extensive information about the human body. The ideal nanobothas not yet been fully comprehended, but when this microscopic robot makes its inevitable debut it will be hailed as a lifesaver by the world of medicine.

- *How do they Work?*

These bots are simply injected in to the body using a syringe. Surgeons will program these minuscule machines depending on the type of task that is needed to be done. There are theories that these bots have a two-way communication system one is through acoustic signals and through sound waves where the external source could reprogram the bots. In the body there could be other bots stationed and report results from the nanobots passing by. Once the task has finished the body can naturally flushed away like the rest of the body's waste.

Nanobots are deployed in to a person's body to apply treatments at the molecular level[1]. On the other hand, Pills could be swallowed which contain molecular robots that deliver medication directly to the area of injury or illness. Machines could be used to target harmful cells or viruses in a person's body and either destroy them or otherwise make them unable to damage a person.

CAPABILITIES:

Nanobots Go Where No Robot Has Gone Before. Surgery's associate risks are not only inherent in the cutting and sewing done by medical staff but include drug-related dangers as well[2]. Patients may be allergic to anesthetics; their organs may become infected from a variety of surgery-related sources; during an organ transplant their body may mysteriously reject the new organ, leading to death; and in the case of a tumor operation, even a few microscopic missed cells can constitute complete failure to battle the cancer[7]. To conquer these conditions we need an effective mechanism that is Nanobots. It is anticipated that they could be equipped with all sorts of tools and cameras in order to furnish more extensive information about the human body. The capabilities of nanobots include their function as:

- Replacement helper-T cells in a weakened immune system
- Ability to interact with materials in their most basic form may enable them to effectively rebuild or "re-grow" damaged tissue.
- Able to remove microscopic particles of cholesterol or cancer, and to rebuild individual molecules to create a new tissue layer.
- In cases where a bone has been broken[2] (researchers have already created a

"nanobone" which has all the properties of natural bone but is also much stronger and more flexible.)

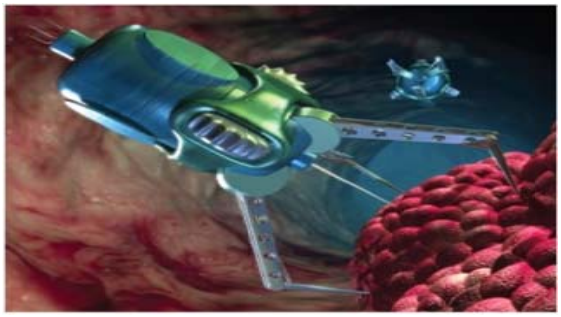


Fig- 1

- Eating away dead flesh at a wound siteto actually re-growing tissue so that it heals cleanly and quickly without leaving a nasty scar.
- Produce synthetic clotting material for their wound sites in order to stop the bleeding.
- Closing a split vein or a gash at the same time.

APPLICATIONS:

The circulatory system is a natural highway for nanomedibots and these will cruise through the blood stream to the area of distress, and are used to attach themselves to specific cells, such as cancer cells, and report the position and structure of these tissues[8]. Nanorobots may also be employed to detect specific chemicals or toxins and could give early warning of organ failure or tissue rejection. Researchers are in progress to develop or to produce light using nanobots (nanophotonics).The fields of Applications are

- To cure skin diseases, It could remove the right amount of dead skin, remove excess oils, add missing oils, apply the right amounts of natural moisturizing compounds, and even achieve the elusive goal of *'deep pore cleaning'* by actually reaching down into pores and cleaning them out[8].
- A mouthwash full of smart nanomachinesremoves pathogenic bacteria while allowing the harmless flora of the mouth to flourish in a healthy ecosystem.
- Medical nanodevices could augment the immune system by finding and disabling unwanted viruses. When an intruder is detected, it can be punctured, letting its contents spill out and ending its effectiveness.
- Devices working in the bloodstream could nibble away at arteriosclerotic deposits, widening the affected blood vessels. This would prevent most heart attacks.

CANCER DETECTION

Nanobots are machines that contain several viable bacteria containing all the required information for combating tumor cells, which are inadequate to defeat cancer. A flagellated non-pathogenic strain of bacterium E.coli carrying extraneous DNA sequence was used to establish communication between nanobots within the blood stream of cancer patients in a computer simulation. Single nanobot that swarm to the target tumor cells has to communicate to other nanobots in the vicinity[2]. It does so by releasing the correctly encoded bacteria that are attracted to the nutrients contained in other nanobots. A more promising tracking method is using an MRI machine to interact with their magnetic nature nanobots are becoming an optimistic type of treatment for cancer. Using an MRI to precisely place the nanomedibots in the cancerous region, the light causes the devices to heat to 131 degrees Fahrenheit which destroys the cancerous cells but doesn't damage surrounding tissues. In cell production, DNA leads **to** messenger RNA **(**mRNA**)** that carries off the instructions for making important proteins. Fire and Mello used particles called small interfering RNAs**,** orsiRNAs, to cut out unwanted pieces of the genetic code in the mRNA of their worm subjects. We can inject nanobots with siRNAs designed to cut out the genetic mutation for cancer in mRNA into the bloodstreams of cancer patients to detect the cancer or to avoid them forming proteins .
Nanobots laden with interfering RNA that deactivates the protein production of the cancer and kills the malignancy would attach themselves to the tumor and deliver the lethal.

GENE THERAPY

In gene therapy using just naked DNA is ineffective. DNA could be embedded into nanoparticles and moved to the desired place in the body and then inserted into cells. Normal DNA is often too large to pass through the cell membrane so special polymers can be used to compact the DNA and allow it to enter the cell. David M.Lynn's team has created a nanoscale film of water soluble polymers and DNA. The films can be coated onto medical devices such as a stent. A stent is used to widen and then support clogged up arteries but smooth muscle can often grow around the stent and make it useless. Coating the stent in this nanoscale film that has DNA with the gene that prevents the smooth muscle growth means the smooth muscle can't grow around the stent and the artery remains open[5].
A problem with gene therapy is that it hard to control the length of time the cells around the stent are exposed to the gene therapy.For thisDavid M.Lynn's team used many layers of DNA and the water soluble polymers. More layers would mean a longer exposure to the gene therapy and also layers of alternative

polymers that take longer to degrade. This means that rather than all the ingredients being simultaneously released in the body, there is a 'soap effect' where the outer layers are slowly degraded away[5]. This 'soap effect' could be particularly useful when using different gene therapy treatments in one. Nanobots insert the DNA into the cells or help in identifying cells and make them highlight to other nanobots equipped for gene therapy. The genes in the cell could be changed slightly to support the addition of the man-made nano-scale materials to create the hybrid cell. The hybrid could then carry out some of functions of nanobot and maybe also enhance the inhabited cells' functions. Such as a T-Lymphocyte could be made to recognise cancer cells and then stimulate the production in hybrid B-Lymphocytes that produce the nanoparticles needed for gene therapy instead of antibodies. These hybrids would be most suitable with blood borne cells as they could exist in the blood and be able to get to any part of the body. They would have the added benefit of not being attacked by the body's immune system because the body would recognise them as their own cells. Stretching a supercoil of DNA between its lower pair of robot arms, the nanomachine gently pulls the unwound strand through an opening in its prow for analysis. Upper arms, meanwhile, detach regulatory proteins from the chain and place them in intake port. The molecular structures of both DNA and proteins are compared to information stored in the database of a larger nanocomputer positioned outside the nucleus and connected to the cell-repair ship by a communications link.

KIDNEYS TREATMENT

Kidney stones can be intensely painful the larger the stone the more difficult it is to pass. Doctors break up large kidney stones using ultrasonic frequencies, but it's not always effective. A nanorobot could break up a kidney stones using a small laser.Nanorobots might carry small ultrasonic signal generators to deliver frequencies directly to kidney stones.

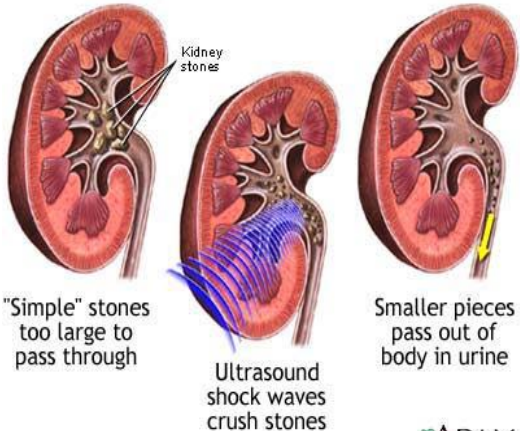


Fig-2

DETECTIONOF ATHEROSCLEROTICLESIONS:

Another significant possible feature of medical nanorobots will be the capability to locate atherosclerotic lesions in stenos blood vessels, particularly in the coronary circulation, and treat them either mechanically, chemically or pharmacologically[4]. Cardiovascular problems are generally correlated with the obesity, human sedentary lifestyle, or hereditary characteristics. Heart problem is the world biggest killer. The Nanorobot Control Design (NCD) is multithread software. It is comprised of collision detection and physically based simulation in addition to removing plaque from arterial walls, they could also be used to find areas of arterial weakness.

Nanorobots could be used to clear built-up cholesterol from your arteries, thereby saving you from a heart attack. If the heart itself is damaged, they work their way up to the affected area and perform micro-surgery that you would probably not feel or notice, but which would almost certainly save your life.

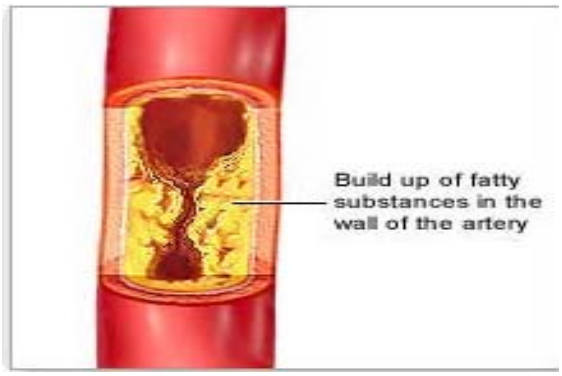


Fig - 3

CONCLUSION:

Nanobots are poised to bring the revolution in medical communitywhich will be the nonhazardous to the living kind.Scientists in the medical field are also predominantly excited about not only the healing nature of nanobots, but also their capacity for research and discovery inside the human body. Nanobots are used to monitor the traffic and better direct it, and alert them to any poisons or dangerous biological substances in our body and track their activitiesand also checks for physiological problems.Their ability to interact with other living systems increases because they can easily cross the skin, lung, and in some cases the blood/brain barriers.Nanobots extends their functionalities in almost all the sectors in today's world like Diagnostics, Drug delivery, Tissue engineering, Catalysis, Filtration, Aerospace, Construction,

Refineries, Consumer goods etc.Since nanorobotresearchers expect to have the first fully functioning prototype released to the public in the next 25 years, the day may soon come when we will have the magnificent experience of seeing ambiances of these Nano-machines.

REFERENCES:

[1]http://www.microscopemaster.com/nanobots.html

[2] http://nanogloss.com/nanobots/how-nanobots-can-repair-damaged-tissue/#axzz275u0xYm4

[3] http://www.ele.uri.edu/courses/ele282/F07/DavidD_1.pdf

[4] "*Nanorobot for Treatment of Patients with Artery Occlusion*" by

Adriano Cavalcanti, Lior Rosen, BijanShirinzadeh and Moshe Rosenfeld

[5] "*How the Nanotechnology used in Gene Theraphy*" By Andrew Simpson

[6] www.wisegeek.com/what-are-nanorobots.htm

[7] www.nanorobotdesign.com

[8] "*Nanorobots:Medicine of the Future*" By AmitBhargava

A REVIEW OF GLOBAL PATH PLANNING ALGORITHMS FOR PLANAR NAVIGATION OF AUTONOMOUS UNDERWATER ROBOTS

[1]DIVYA KONDA, [2]DIVYA KONDA & [3]S. SARAVANAKUMAR

[1&2]Department of ICE, National Institute of Technology,Tiruchirapalli, India
[3]Engineering Design Department,Indian Institute of Technology Madras, Chennai, India
Email: divk1991@gmail.com, keerthana1991@gmail.com, srsaravanakumar@gmail.com

Abstract— Path planning is one of the most important navigation schemes of any autonomous robot. The time complexity of the algorithm and the length of the path generated determine the quality of the algorithm. Hence it is necessary to select a proper algorithm for better path planning of a robot. This paper provides a survey of the global path planning methods for Autonomous Underwater Robots (AUR). The algorithms are developed in C++ language and the generated paths are shown using MATLAB environment. In order to analyze, the efficiency of the algorithm for global path planning, various mazes and conditions are considered. The time complexity by means of the number of clock cycles taken for the completion of the program execution is calculated for each algorithm. The various algorithms and the simulations results are presented in detail.

Keywords- *AUR, path planning, time-complexity, grid based, maze*

I. INTRODUCTION

Path planning is basically a path selection process performed by robots to take a safe route to avoid obstacles and find a safe and optimal path between two points. Based on the information availability from the environment there are two types of path planning methods: global and local path planning. If the environment is pre-known, it is called as global path planning and the path planning in unknown environment is called as local path planning [1], [2]. It is also classified as off-line or static and on-line or dynamic path planning based on the behavior of the obstacles. If the path is a predefined decision in the case of static obstacles, then the path planning is called offline decision making or static path planning. If the decisions are made by the robots when the obstacles are not stationary (moving obstacles), then the situation is known as on-line or dynamic path planning [3].

Path planning is success only if the path is generated in minimal time. The path taken is said to be optimal on a condition that an objective function such as distance travelled is less within the time stipulation. Path planning is been an ongoing process in the field of research that each and every existing algorithm is being constantly reviewed and improved. It can be performed by different algorithms which help in deciding the optimal solution [4]. Path planning algorithms are classified as Grid based algorithms, Geometric algorithms, Potential field and Sampling based algorithms [5], [6]. Grid based algorithms are used for low dimensional workspaces. In these algorithms, the entire space is considered as the coordinate space mapping of the x and y coordinates. The minimal path is chosen based on the objective (cost) function. Geometric algorithms are the algorithms in which the robots are considered as points among polygonal obstacles. Potential field based algorithms consider the robot as a point object which shows an attractive force towards the goal point and repulsive force against the obstacles. In sampling based algorithms, the entire robot's environmental space is divided into N samples. The samples which are considered as free of obstacles are called milestones. Connections are established between the different milestones to obtain the path towards the goal.

In this paper, the grid based algorithms such as wall following, breadth first search, depth first search, A*, Dijkstra's are reviewed for off-line (global) path planning of AUR. It is assumed that the obstacles are stationary and present in the form of maze. A maze is a confusing intricate network of passages. Mazes can be classified into perfect, braid, unicursal and sparse mazes based on routing. In our work a perfect maze is considered for path planning by obstacle avoidance. A perfect maze, otherwise called simply-connected maze, is a maze without any closed circuits or inaccessible paths. The path planning algorithms can be implemented to find the optimal path towards the destination. Here the optimal path is selected based on the length of the path and the number of cycles taken for generating the path. Each algorithm is given revisit in this paper to solve different cases of obstacles given in form of mazes. The simulations are carried out and the results are discussed in detail. The simulation time for each algorithm is been calculated and results have been compared. The algorithms were coded in C++ language and the results are mapped using MATLAB. The AUR is considered as a point moving in 2D space. In order to study the motion of actual AUR, a virtual simulator using the 3D model of the actual robot can be used [7].

The rest of the paper is organized in three sections. In Section II, the different types of off-line path planning algorithms are described. Section III consists of simulation results and the discussions of the reviewed algorithms. Finally, the conclusion and future work are given in Section IV.

II. OFF-LINE PATH PLANNING ALGORITHMS

The different algorithms which have been detailed are wall following, breadth first search, depth first search, A*, dijkstra's. The maximum time taken to complete the simulation considering the worst case is known as time complexity. The run time of the each code is based on the length of the code and the size of the inputs. Run time analysis is required to examine the efficiency of the algorithm. The comparative results have been obtained for the same maze and scrutinized the simulation time for each algorithm. Space complexity is another factor which has to be considered in evaluating the efficiency of different algorithms. Space complexity is the amount of memory space required for the program storage.

A. Wall following algorithm

The wall following algorithm is one of the easiest algorithm to solve a simply connected maze. A wall following algorithm can be either left wall following or right wall following. The pseudo code for a left wall following algorithm is as follows.

```
When the robot enters a cell,
Check for a left wall
        If there is a left wall,
        Check for front wall
                If there is a front wall
                Check for a right wall
                        If there is a right wall
                        Turn around
                        Else (if there is no right
wall)
                        Turn right
                Else (if there is no front wall)
                Go front
        Else (if there is no left wall)
        Go left
```

Right wall following follows the wall with the wall at the right side of the robot. The major disadvantage of the wall-following algorithm is that it cannot be used for mazes that are not simply connected.

B. Breadth first search (BFS) algorithm

Breadth first search algorithm is one of the algorithms that are used for effective maze-solving and path planning in mobile robots. It is an uninformed algorithm i.e. it does not use any information about how far the robot is from the goal or how far the robot has travelled. BFS algorithm searches a graph breadth-wise and checks every node that can be a potential goal point. A queue (FIFO) is used to store all nodes of the graph which has to be traversed. The information about obstacles and walls is fed in prior to applying the algorithm.

Breadth-first search algorithm allows the control to traverse through most of the nodes of the graph before finding the optimal path and thus results in the shortest solution in a maze. Breadth first search operates by expanding each node by queuing the allowed neighboring cells of the node in the graph. At first, the queue contains only the root node, which is the start point of the robot, and in each iteration, the node is removed and expanded i.e. the allowed neighbors of the node are queued. The child nodes of the expanded node that are not queued include those where obstacles are placed and also the nodes that were already visited in the past. This process of subsequent queuing and dequeuing is done till the goal point is encountered. When the control reaches goal point, the nodes that lead to the goal point are traced back thus giving a path from the starting to the goal point. The advantage of the BFS algorithm is that it never fails to find the path if one exists. Also, if more than one path exists, the shortest path is chosen in the maze. The disadvantage of the algorithm is that it consumes a lot of memory compared to the other algorithms as it stores all the nodes of the graph.

C. Depth first search (DFS) algorithm

Depth first search algorithm is a graph search algorithm which goes deeper into the graph. It is similar to the breadth first search in operation but uses a first-in-last-out stack to contain the nodes. It expands the nodes by popping the last-added node and pushing its unvisited allowed neighbors into the stack and repeating the popping of the next node thus traversing the depth of the graph till the goal point is reached. Once the goal point is reached, the path is traced to the start point. The advantage of the DFS algorithm is that it consumes lesser space when compared to breadth first search algorithm. It is time-limited rather than space-limited. The disadvantage of the algorithm is that it may not always result in an optimal path, if more than one solution exists. Moreover, there is no guarantee that a solution will be found when DFS is used.

D. A algorithm*

This algorithm is the best algorithm in finding the goal point in the minimum path based on the heuristic cost function. This algorithm finds the best and the shortest path for predefined start and goal points. The heuristic cost function is calculated based on the distance and the directional priority. The A* algorithm transverses the nodes which consists of shortest path in their way by placing the nodes visited into the priority queue in sorted form. Total cost function which helps in deciding the path to be taken is based on two factors. Cost function can be defined of the form $f(x) = g(x) + h(x)$,where $f(x)$ is the total cost function, $g(x)$ is the path-cost function from the starting point to the current node and $h(x)$ is an admissible heuristic function from the current point to the goal point. One of the factors involves path cost which is a cost function from the starting point to the current position. The other factor is the heuristic estimate from current position to the goal position. Other graph algorithms such as Dijkstra's and depth first search (DFS) can be implemented based on the concepts of A* algorithm implementation. Each node transverse maintains a pointer to the parent node so that when the best path is chosen, it can easily be

traced back. A* start algorithm basically has an open as well as closed list. The visited nodes is saved on to the closed list such that each time a new node is considered for cost function calculation, the closed or visited nodes are ignored. The open list consists of all the nodes yet to be visited.

E. Dijkstra's algorithm

Algorithm is a graph search algorithm which obtains the shortest path for a graph with non negative edge path cost. It is a greedy algorithm. This algorithm is based on uniform cost function. This can be viewed as a special case of A* algorithm. It follows the exact same cost function f(x). The only difference between generalized case of A* algorithm and Dijkstra's algorithm is that heuristic function, $h(x) = 0$. The algorithm of Dijkstra's is as follows:

1. Every node is assigned a temporary initial value of zero.
2. All nodes are considered to be unvisited and current node is the initial node.
3. All the unvisited nodes of the current node are considered and distances cost is calculated. If distance of any particular node with current node is less than the previous, that distance is overwritten to path-cost function $g(x)$.
4. After considering all the neighbors, mark the current node as visited and move on to the next node decided based on the minimum total cost function.
5. When the destination node is visited, the algorithm is a success and the path with minimal total cost function is traced back.
6. If the destination is unvisited, the current node has to be analyzed so repeat step 3.

III. RESULTS AND DISCUSSION

In order to study the performance of the above discussed algorithms, numerical simulations are carried out. Simulations are performed for three cases. Case-I deals with maze solving abilities of the algorithms whereas Case-II deals with the limitations of wall following algorithms. Case-III deals with comparison between BFS and DFS algorithms.

A. Maze solving – A comparison

Fig. 1 illustrates the maze used as obstacles for the above discussed algorithms. This maze is taken in such a way that there exists many paths between the initial and end. The starting and goal positions are located at (02,20) and (19,01) respectively. The simulations are done by pre-loading the static obstacle positions in Dev C++ and plotting the obtained coordinates using MATLAB plots. The paths generated by the algorithms are shown in Fig. 2. It can be seen that the algorithms are capable of solving mazes. It has been observed that the wall following and depth first algorithms generates longer path. The path generated in BFS, A* and Dijkstra's are shorter and almost over lapped.

The algorithms are compared with each other in terms of time complexity and the length of the path generated in order to find out the efficiency of each algorithm. Table 1 gives the number of cycles taken for execution of code for each algorithm and also the length of the path found by each algorithm. From the table, it can be inferred that A* and Dijkstra's can be preferred over others as far as time complexity is concerned. The BFS and Dijkstra's algorithms resulted in the shortest path closely followed by the A* algorithm. Hence it can be said that Dijkstra's algorithm generates optimal path.

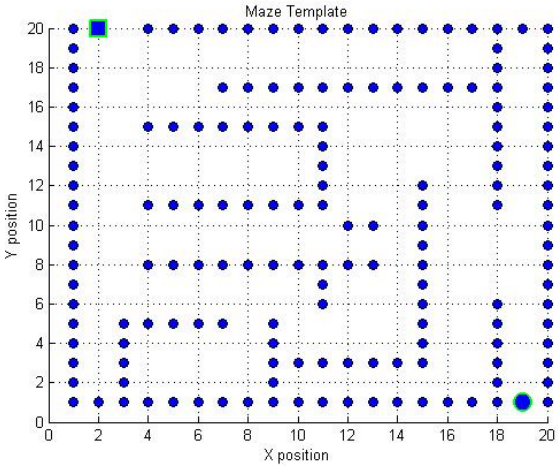


Figure 1. The perfect or simply-connected maze.

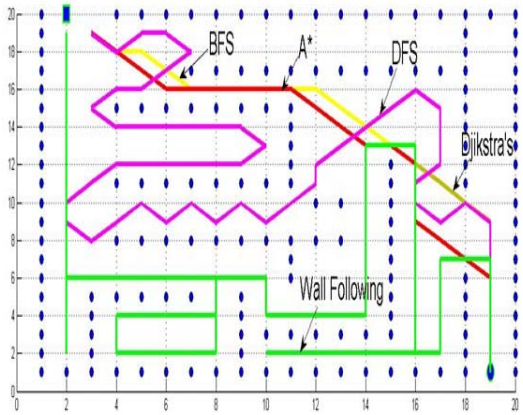


Figure 2. Comparison of paths generated by different algorithms

TABLE 1. COMPARIOSIN OF TIME COMPLEXITY OF THE ALGORITHMS

Algorithm	**No. of cycles**	**Length of path**
Wall Following	51	99
Breadth First Search	59	28.14
Depth First Search	58	68.43

A*	35	29.79
Dijkstra's	33	28.14

B. Maze solving by wall-following algorithm

Wall following algorithm is, with no doubt, efficient in finding a path through a simply-connected maze with no extra usage of memory. However, this method may not always find the shortest path through the maze. Also, it fails to find a path when a closed circuit is present in the path. This limitation of the wall following algorithm is demonstrated by taking an example of a maze as shown in Fig 3. It can be observed that the algorithm leads the control to eventually return back to the same starting point and go in loops, thus not reaching the goal point. The robot goes in loops around the U-shaped continuous wall and fails to reach the goal point as desired.

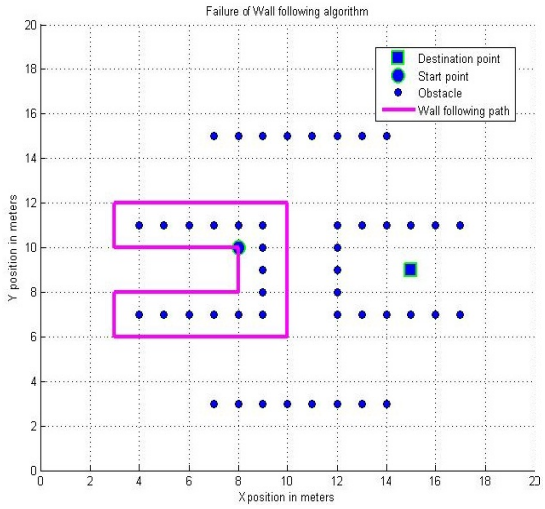


Figure 3. Failure of wall following algorithm due to presence of a closed circuit

C. Breadth first search(BFS) and depth first search(DFS) – A comparison

Breadth first search (BFS) algorithm uses a queue for saving the nodes of the root while depth first search (DFS) uses a stack for saving the nodes of the root. This changes the comfort direction of the path chosen by the algorithms while tracing a path from a starting point to a goal point in an open space. The breadth first search gives the shortest path when the goal point is along the breadth from the starting point. The depth first search gives the shortest path when the goal point is along the depth from the starting point. The difference has been observed in two cases for the given same maze. In Case-A, the starting and goal positions are given at (1,1) and (1,20) where as they are specified at (1,I) and (20,1) respectively. Fig. 3 illustrates the Case-A. In this case the depth first search traces the shortest path while in Case-B the breadth first search traces the shortest path. The length of the path calculated for both cases are shown in Table 2 and 3. It has been clear that if the path to be required is along the x-axis then the .breadth first method can be selected. Similarly if the path to be required is along the y-axis then the depth first search can be preferred

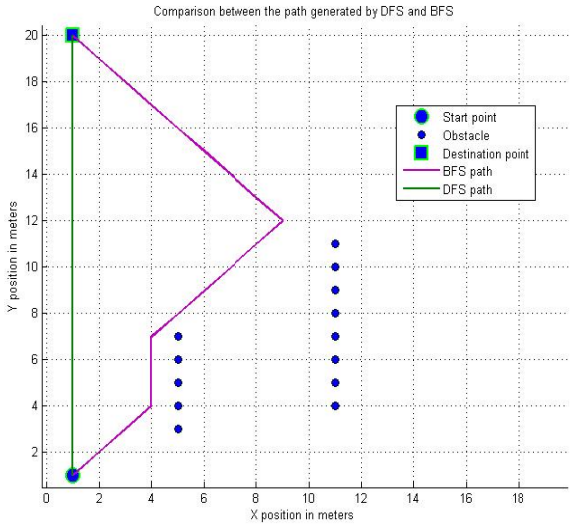


Figure 4. Shortest path generated by DFS algorithm

TABLE II. COMPARISON OF PATH LEGTNS FOR CASE -A

Algorithm	Length of the path
Breadth first search (BFS)	25.63
Depth first search (DFS)	19

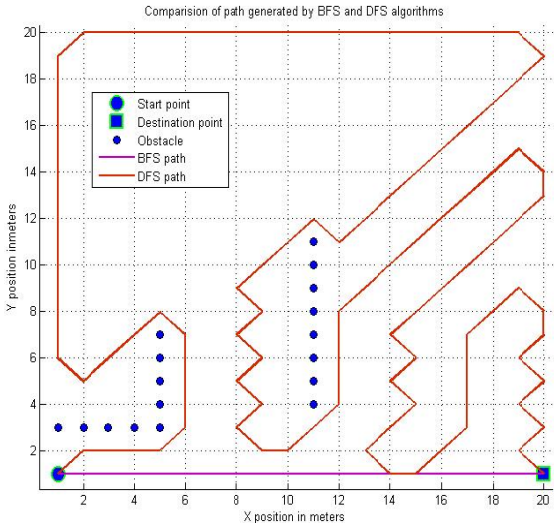


Figure 5. Shortest path generated by BFS algorithm.

TABLE III. COMPARISION OF PATH LENGTHS FOR CASE-B

Algorithm	Length of the path
Breadth first search (BFS)	19
Depth first search (DFS)	135.27

IV. CONCLUSIONS AND FUTURE WORK

The different types of algorithms for global path planning of AUR have been discussed in this paper. The generated x and y co-ordinates with C++ programming language are interfaced are plotted using MATLAB in order to visualize the path generated by the algorithms. It has been observed that A* and Dijkstra's algorithms consume less time and therefore are most preferred algorithms compared to the others. BFS and DFS algorithms consumer more time compared to the above mentioned two. Wall following is the simplest algorithm but it is in danger of falling into bottlenecks. The cases of failure of wall following algorithm and maximum efficiency of breadth first search and depth first search algorithms are discussed and illustrated with different cases. To improve the visual aesthetics of the user interface and to study the motion behavior of the AUR, the algorithm can be interfaced with a virtual reality simulator. In this regard, a virtual simulator for flat-fish shape AUR has been already developed. The above discussed algorithms will be interfaced with virtual simulators and the results will be presented in near future.

V. REFERENCES

[1] J. C. Latombe, Robot Motion Planning, MA: Kluwer Academic, Norwell, 1991.

[2] M. G. Park and M. C. Lee, "A New Technique to Escape Local Minimum in Artificial Potential Field Based Path Planning," KSME Int. Journal vol.17, pp. 1876–1885, 2003.

[3] T.H.Cormen, C.E. Leiserson and R.L. Rivest, Introduction to Algorithms, McGraw-Hill Book Company, 1990.

[4] P.Raja and S.Pugazhenthi, "Optimal path planning of mobile robots: A review," International Journal of Physics, vol. 7(9), Feb., 2012, pp. 1314-1320.

[5] D. Henrich, "Fast motion planning by parallel processing- A review," Journal of intelligent and robotic systems, vol 20, No 1, Sept.1991, pp 45-69

[6] S. M. LaValle, Planning Algorithms, Cambridge University Press, NewYork, 2006

[7] S.Saravanakumar, Divya Konda, B Keerthana and T Asokan, "3D Modeling and Virtual Simulator for a Flat-fish Shaped Autonomous Underwater Vehicle," Proc 2nd Int. Nat. Conf. on Simulation, Modelling, and Analysis (COSMA), Dec. 2011, pp. 385-390, Coimbatore.

A NEW CONCEPT IN BLUETOOTH COMMUNICATION

C.VAMSI VARSHIKA & R.NAGENDRA

Sri Vidyanikethan Engineering College (Autonomous status by the UGC)
Sree Sainath Nagar, Tirupati, A.Ranganpet, Andhra Pradesh

Abstract—Bluetooth communication is an emerging wireless network. Its characteristics are wireless, openness and had the low power. To increase the security in data transmission a new concept in Bluetooth communication is employed. Currently stream cipher E0 is employed. Currently stream cipher E0 is implemented. To increase the security level of data transmission a new concept in Bluetooth communication is proposed.

Keywords-*Bluetooth; E0 key stream; encryption algorithm; data transmission*

I. INTRODUCTION

Bluetooth technology is an emerging wireless networking standard, which is based on chip that provides short-range wireless frequency hopping communication. Now, Bluetooth technology is mainly applied to the communication between mobile terminal devices, such as palm computers, mobile phones, laptops and so on, and also can successfully simplify the communication among above devices and the Internet, so that the data transmission between these modern communication equipments and Internet has become more quickly and efficiently, and widen the road for wireless communications. It has the characteristic of wireless, openness, low-power and so on. However, the phenomenon of data-leaking frequently arise in using the Bluetooth technology for data transfer, since the emergence of Bluetooth, even if the Bluetooth takes the very robust security measures, there are still serious security risks. encryption process is the E0 stream cipher. However, this algorithm has some shortcomings, 128-bit E0 stream ciphers in some cases can be cracked by 0 (2^{64}) mode in some cases. So, for most applications that which need to give top priority to confidentiality, the data security is not enough if only use Bluetooth. Now I will introduce the Bluetooth mechanism, its disadvantages, and then propose a hybrid encryption algorithm to solve the current security risk in Bluetooth data transmission.

II. THE ENCRYPTION ALGORITHM IN BLUETOOTH SECURITY MECHANISM

A. Bluetooth security mechanism

The Bluetooth specification defines three security modes:

1) Safe Mode 1: No safe mode, which has the lowest security level;

2) Safe Mode 2: service-oriented security model, which start after the establishment of the channel;

3) Safe Mode 3: link-oriented security model, which install and initial before communication link is established.

Bluetooth system provides safety precautions in the application layer and link layer, the two sides achieve authentication and encryption in the same way. Link layer uses four entities to ensure the safety:

1) *48-bit of the Bluetooth device address, which is global uniqueness decided by the IEEE;*
2) *The authentication key for entity authentication is 128-bit;*
3) *The secret key for data encryption is 8 ~ 128-bit;*
4) *128-bit random number trades once, changes once.*

Two keys are generated in the initialization process and do not open, encryption key is generated in the certification process from the authentication key, but it is different from the authentication key, every time when you activate the encryption, it will generate a new secret key. Authentication key is more stable, after generating,, it is decided by the concrete application of Bluetooth device whether to change . The random numbers of Bluetooth demands "random generation" and "non-repeatability", that is to say the random numbers are almost impossible to duplicate and can not be significantly greater than zero probability estimate of the random numbers in the authentication key life. Now, Applying linear congruential generator to generate random numbers is widely adopted at present, its expression is as follows:

$$X_n + 1 = a * X_n + c \pmod{k} \quad n \geq 0, \quad (1)$$

Where a, c are constants, k is the mold, we generate a series of random numbers taking a certain number of X0 for seed number.

B. Authentication and encryption process of Bluetooth

Bluetooth security-mechanism is divided into three modules including key generation, authentication and encryption, and adopt four kinds of algorithms as E0 E1, E2, E3. Bluetooth system provides authentication, encryption and key management functions in Link layer. PIN code was entered by the user, by means of the E2 algorithm for generating the link key, by means of E3 algorithm, getting encryption key, make use of E0 algorithm generated key stream, and encrypt plaintext, then get cipher text. Figure 1 is the process of Bluetooth

encryption.

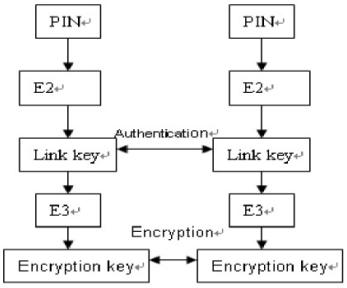


Figure 1. The process of Bluetooth encryption.

The three modules of Figure 1 are as follows: 1) key generation module, algorithm E2 is used for generating the link key, and its input parameter is a 4-digit passwords number which is entered by the user, the algorithm E3 calculates encryption key KC by the use of E2 link key encryption key as input parameters. 2) Encryption module, algorithm E0 can be used for generating keys stream to encrypt the original data. 3) Authentication module, algorithm E1 is the crucial algorithms in the authentication process, the two units in need of certification use each authentication algorithm E1 to generate identification word and compare, then complete certification.

C. Analysis of E0 Algorithms

E0 algorithm is the encryption algorithms in Bluetooth link layer, which belongs to stream encryption method, that is to say it take data flow and the key bit stream Exclusive-or operation. The payload of each packet is encrypted separately, and the encryption occurs before MPE-FEC, after the cyclic redundancy check. The main principle is to use linear feedback shift register to generate pseudo-random sequence, after that form key stream that can be used for encryption, and then take the key stream and data stream that need encryption Exclusive-or operation, and achieve encryption. During decryption, the cipher text take Exclusive-or operation once more, re-plaintext can be obtained.

III. HIDDEN DANGER OF BLUETOOTH SECURITY SYSTEM

A.The weakness of E0 stream cipher algorithm

The main weakness of Stream cipher algorithm is that if a pseudo-random sequence make an error, it will make the whole cipher text mistake happen, it also bring about the cipher text can not restore back to plaintext in decipherment.

The security of Stream cipher algorithm system relies on the internal mechanism of the secret key stream generator solely. If its output is endless sequence of 0, then the cipher text is the plaintext, so that the whole system is worthless; if its output is a periodic 16-bit mode, then the algorithm is only an Exclusive-or operation which can ignore security; if the output is a series of endless random sequence (which is truly random, non-pseudo-random), then there is one-time pad and very perfect safety. The security of actual stream cipher algorithm depends on a simple Exclusive-or operation and the one-time pad.

Key stream comes from Key stream generator, seemingly random, but the fact is certain, it can reappear well in the decryption. Secret keys that output from key stream generator output is the closer to random, it is much harder for the cryptanalyst. However, this random key stream is not acquired easily.

B. Limited resources capacity of linear feedback shift register LFSR

Encryption algorithm used in Bluetooth technology standard is somewhat fragile, and even if its E0 stream cipher uses 128-bit key, in some cases, the complexity of their decoding is only 0.

There are 4 LFSR in key stream generator of E0 stream cipher. If a certain LFSR of the key stream generator generated a sequence of cycle is shorter than the key, there is the threat from attacker divide and conquer. And the efficiency of LFSR software implementation is very low. In the implementation procedure, it is needed to avoid the sparse feedback polynomials, because they are easy to face correlative attack, but the thickset feedback polynomial are very ineffective. In fact, the software implementation of LFSR algorithm is not faster than the DES and RSA hybrid encryption algorithm.

C. Low credibility of PIN

Bluetooth technology uses non-standard 4 -digit PIN code and another variable to generate the link key and encryption key. Actually, 4-digit PIN code is the only variable which is the real key generated, resulting only one key (a random number) transport in the air.

In the process of Creating a link key, intruder intercepts the communication data packet in the first communication process. In order to derive a variety of relevant parameters, including the link key, try brute force attack on the PIN. Here brute force attack is exhaustive key search, if the PIN is k bits, then only in the case of cipher text attack, an attacker can search the value of the PIN through 2k times. Therefore, the credibility of the PIN code is lower, 4 bits PIN code only has 10,000 possibilities. One solution is to choose and use 16-byte PIN code, or use the public key system. If using a longer PIN code can increase the based on the difficulty of attacker get encryption keys,but its really inconvinent.because everytime when secure connection is established, we should have to enter a PIN code.

D. High probability of non-link key cheat

Along with the use of the link key takes new problems. Authentication and encryption set up on the basis of the link key. All the other Information used in this connection usually is public. However, this will lead to the following questions:

1) Device A and B using the secret key of device A as the link key.

2) At the sanme tme or later ,device C may communicate with the device A and use the key of device A as their link key.

3) Device B can use the link key of device A to decrypt the communication information between device A and device C.

As discussed above, device B which get the key of device A can use this key with one camouflaged BD-ADDR to calculate the encryption key, then achieve monitoring device A to communicate with other devices.

And the device B can disguise device C through device A certifies, also can disguise device A through device C certifies.

E. Address Spoofing

Every Bluetooth device has a unique Bluetooth device address. However, its uniqueness raises new problems. Once the ID links with a certain fixed person, this person can be tracked and their activities can easily be recorded. In this case, the individual's privacy will be violated.

Above these problems can lead people to believe that the Bluetooth security system is highly unreliable, but there is a fact can not be ignored is that: in general, the data transmitted via Bluetooth connection is not very important. Now, Bluetooth standard is only applicable in smaller networks because considered security technology, if the network nodes are more complex and multiple, the existing key distribution and authentication based on point to point can not meet the demand. Bluetooth technology provides data security measures for small-scale applications appear to be enough, but any sensitive data or the data that may cause problems should not be transferred via Bluetooth directly. In order to uses Bluetooth technology more widely, we can use other more powerful encryption algorithms, such as DES and RSA hybrid encryption algorithm.

IV. THE IDEAS AND PROCESSES OF HYBRID ENCRYPTION ALGORITHM

RSA algorithm is the first relatively complete public key algorithm. It can be used for data encryption, also can be used for digital signature algorithms. RSA cryptosystem is based on the difficulty of factorization in the group Zn and its security establishes in the assumption that constructed by almost all the important mathematicians, it is still a theorem that does not permit, which is lack of proof, but Mathematicians believe it is existent DES is a group cipher algorithm,which encrypts data by a group of 64-bit.A group of 64-bit plaintext is entered from one beginning of the algorithm, 64-bit cipher text is exported from the other side. DES is a symmetric algorithm, encryption and decryption use the same algorithm (e the different key arrangement), the key can be any 56-bit value (the key is usually 64-bit binary number, but every number that is a multiple of 8-bit used for parity are ignored). this algorithm uses two basic encryption techniques, make them chaos and spread, and composite them.

Seeing from the efficiency of encryption and decryption, DES algorithm is better than the RSA algorithm. The speeds of DES encryption is up to several M per second, it is suitable for encrypting large number of message; RSA algorithm is based on the difficulty of factoring, and its computing velocity is slower than DES', and it is only suitable for encrypting a small amount of data, The RSA encryption algorithm used in the. NET, it encrypts data at most 117 bytes of once.

Seeing from key management, RSA algorithm is more superior than the DES algorithm. Because the RSA algorithm can distribute encryption key openly, it is also very easy to update the encryption keys, and for the different communication objects, just keep the decryption keys secret; DES algorithm requires to distribute a secret key before communication, replacement of key is more difficulty, different communication objects, DES need to generate and keep a different key.

Based on the comparison of above DES algorithm and RSA algorithms, in order to give expression to the advantages of the two algorithms, and avoid their shortcomings at the same time, we can conceive a new encryption algorithm, that is, DES and RSA hybrid encryption algorithm. We will apply hybrid encryption algorithm to Bluetooth technology, we can solve the current security risks of Bluetooth technology effectively.

The entire hybrid encryption process is as follows: Let the sender is A, the receiver is B, B's public key is e_B, B's private key is d_B, K is DES encryption session key (assuming that the two sides of communication know each RSA public key).

A. Process of encryption

During the process of sending encrypted information, the random number generator uses 64-bit DES session key only once, it encrypt the plaintext to produce cipher text. On the other hand, the sender get debit's public key from public key management center, and then using RSA to encrypt session key. Finally, the combination of the session key from RSA encryption and the cipher text from DES encryption are sent out.

DES encryption scheme is that encrypt the plaintext bit-by-bit or byte-by-byte, then form key stream, and the intermediate processing results are saved in the process. Key stream has the characteristics of self

synchronization.if the key text which is sent encounter errors and data lost.it will affect a small section of the final text(64-bit).It is different from Bluetooth stream. cipher algorithm.Cellular message encryption algorithm is mathematically prove.

The first, DES algorithm encrypts Bluetooth data packet:

1) Bluetooth packet plaintext M is divided into 64-bit plaintext Mi(i=1,2,…,n)).

2) Crypts Mi for 16 cycles by 64-bit key K ,and Mi will turn into a 64-bit cipher text Ci (i = 1,2, ... n), then all the

Ci (i = 1,2 , ... n) are combined into cipher text C.

The second, RSA algorithm encrypts the key of DES algorithm:

3) Obtain RSA public key of receiver B from the key server, or other sources.

4) Make DES 64-bit session key K for RSA encryption by public key e_B that obtains from recipient, then a session key encrypted information CK is formed

5) Composite Cipher text message C from the use of DES encryption, and session key CK from RSA encryption,

we can get the hybrid CM for transmission. Figure 2 is the

whole mixed-encryption process.

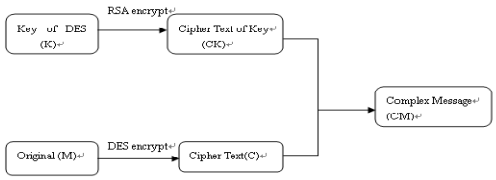


Figure 2. The whole mixed-encryption process.

B. Process of decryption

The decryption of hybrid encryption algorithm is as follows. The first, the receiver B divide received cipher text CM into two parts, one is cipher text CK from the RSA algorithm encryption, the other is cipher text C from the DES algorithm encryption. The second, the receiver B decrypt cipher text CK by their own private key dB,receive the key K which belongs DES algorithm, then decrypt the cipher text C to the original M by key K. Figure 3 is a decryption of hybrid encryption algorithm.

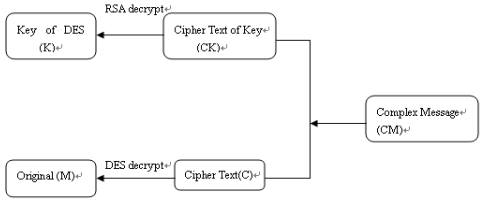


Figure 3. A decryption of hybrid encryption algorithm.

C. The advantages of hybrid encryption algorithm

Using RSA algorithm and the DES key for data transmission, so it is no need to transfer DES key secretly before communication;

Management of RSA key is the same as RSA situation, only keep one decryption key secret;

Using RSA to send keys, so it can also use for digital signature.

The speed of encryption and decryption is the same as DES. In other words, the time-consuming RSA just do with DES keys.

D. Safety analysis of hybrid encryption algorithm

Safety of Hybrid encryption algorithm is based on the safety of RSA algorithm and DES algorithm, operating efficiency of hybrid encryption algorithm depends on the speed and high efficiency of encryption and decryption by DES algorithm. Of course, the Bluetooth based on hybrid encryption algorithm, its data transmissionsecurity depend on the security of hybrid encryption algorithm. DES key space is 256, the hardware decoding speed is fairly rapid. In 1997, people used DES decryption special machines to break DES algorithm, it just need six hours to break. Therefore, 56-bit DES key has clearly affected the strength of its confidentiality. Moreover, DES algorithm is completely open, it is not suitable for exclusive use in a networked environment. At present, RSA encryption algorithm is a kind of more successful public key cryptosystem in theoretical and practical application, and its security is based on the difficulty of large integer resolution into prime factors. And its security depends on the large integer factorization, but whether it is equivalent to large integer factorization has not been proven in theory, because there is no proof of cracking.RSA will definitely need to make large integer factorization.

As long as we protect the key that encrypt original, and the security of entire file will be guaranteed. Because of the dual protection of DES algorithm and RSA algorithm, the data in transit is safe.

V. CONCLUSIONS

Currently, stream cipher E0 used in Bluetooth standard has many shortcomings. While the DES and RSA hybrid encryption algorithm is relatively more secure and easier to achieve. Thus ensures data transmission between the Bluetooth device safely and in real-time.

REFERENCES

[1] Zheng Hu. Network and Information Security [M]. Peking: Tsinghua University Pres,2006.

[2] Man Young Rhee. Network Security Encryption Principle, algorithm and Protocol[M]. Peking: Tsinghua University Pres, 2007.

[3] Suri , P. R . ; Rani , S. Bluetooth security Need to increase the efficiency in pairing [J]. IEEE/ Southeastcon , 2008.

[4] Fengying Wang. Dynamic Key 3DES Algorithm of Discrete System Based on Multi-dimension Chaos[J]. Microelectronics and Computer, 2005, 7: 25-28.