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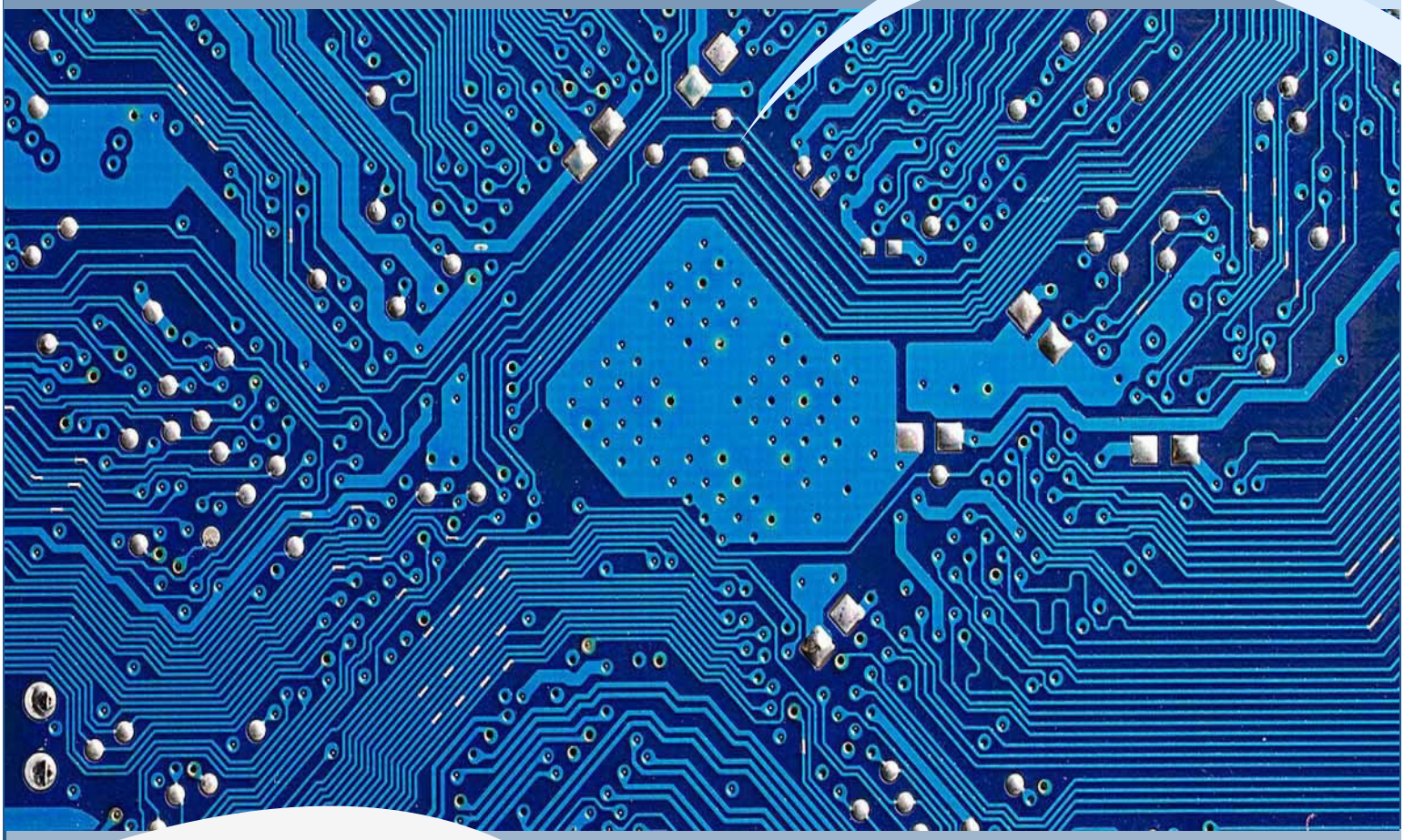

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Editorial

Although the discipline like electrical engineering has narrated academic maturity in the last decades, but the limitations of the non renewable energy sources, turbulence and disturbances in the energy propagation cascades various insightfulness and stimulation in post classical electrical era. Evidence shows that there are phenomenal supplements in power generation and control after the introduction of Energy Management System (EMS) supported by Supervisory Control and Data Acquisition (SCADA). As there is increasing focus on strengthening the capacity of the power houses with the existing resources or constraints some new dimensions like FACTS, Optimal System Generation, High Voltage DC transmission system, Power Generation Control, Soft Computing, Compensation of transmission line, Protection scheme of generator, Loss calculation, economics of generation, fault analysis in power systems are emerging. Since the world is suffering with water, food, and energy crisis, energy consumption has social relevancy.

Keeping view of the ongoing energy and power issues many action research can be initiated by the research fraternity of this domain. The conference is a thought provoking outcome of all these interrelated facts.

In the quest of making this earth a better place to live we have to make a strong hold upon sustainable energy source. Sustainable energy sources include all renewable energy sources, such as hydroelectricity, solar energy, wind energy, wave power, geothermal energy, bioenergy, and tidal power. It usually also includes technologies designed to improve energy efficiency. Energy efficiency and renewable energy are said to be the twin pillars of sustainable energy. Renewable energy technologies are essential contributors to sustainable energy as they generally contribute to world energy security, reducing dependence on fossil fuel resources, and providing opportunities for mitigating greenhouse gases.

Let me highlight some of the recent developments in Electronics discipline. The new integrated devices did not find a ready market. Users were concerned because the individual transistors, resistors, and other electronic circuit components could not be tested individually to ensure their reliability. Also, early integrated circuits were expensive, and they impinged on the turf that traditionally belonged to the circuit designers at the customer's company. Again, Bob Noyce made a seminal contribution. He offered to sell the complete circuits for less than the customer could purchase individual components to build them. (It was also significantly less than it was costing us to build them!) This step opened the market and helped develop the manufacturing volumes necessary to reduce manufacturing costs to competitive levels. To this day the cost reductions resulting from economies of scale and newer high-density technology are passed on to the user—often before they are actually realized by the circuit manufacturer. As a result, we all know that the high-performance electronic gadget of today will be replaced with one of higher performance and lower cost tomorrow.

The integrated circuit completely changed the economics of electronics. Initially we looked forward to the time when an individual transistor might sell for a dollar. Today that dollar can buy tens of millions of transistors as part of a complex circuit. This cost reduction has made the technology ubiquitous—nearly any application that processes information today can be done most economically electronically. No other technology that I can identify has undergone such a dramatic decrease in cost, let alone the improved performance that comes from making things smaller and smaller. The technology has advanced so fast that I am amazed we can design and manufacture the products in common use today. It is a classic case of lifting

ourselves up by our bootstraps—only with today's increasingly powerful computers can we design tomorrow's chips.

The mushrooming growth of the IT industry in the 21st century determines the pace of research and innovation across the globe. In a similar fashion Computer Science has acquired a path breaking trend by making a swift in a number of cross functional disciplines like Bio-Science, Health Science, Performance Engineering, Applied Behavioral Science, and Intelligence. It seems like the quest of Homo Sapience Community to integrate this world with a vision of Exchange of Knowledge and Culture is coming at the end. Apparently the quotation "Shrunken Earth, Shrinking Humanity" holds true as the connectivity and the flux of information remains on a simple command over an internet protocol address. Still there remains a substantial relativity in both the disciplines which underscores further extension of existing literature to augment the socio-economic relevancy of these two fields of study. The IT tycoon Microsoft addressing at the annual Worldwide Partner Conference in Los Angeles introduced Cloud ERP (Enterprise Resource Planning,) and updated CRM (Customer Relationship Management) software which emphasizes the ongoing research on capacity building of the Internal Business Process. It is worth mentioning here that Hewlett-Packard has been with flying colors with 4G touch pad removing comfort ability barriers with 2G and 3G. If we progress, the discussion will never limit because advancement is seamlessly flowing at the most efficient and state-of-the art universities and research labs like Laboratory for Advanced Systems Research, University of California. Unquestionably apex bodies like UNO, WTO and IBRD include these two disciplines in their millennium development agenda, realizing the aftermath of the various application projects like VSAT, POLNET, EDUSAT and many more. 'IT' has magnified the influence of knowledge management and congruently responding to social and industrial revolution.

It's my pleasure to welcome all the participants, delegates and organizer to this international conference. In the process of organizing this conference IRNet family members have shown their commitment and dedication. I sincerely thank all the authors for their invaluable contribution to this conference. I am indebted towards the reviewers and Board of Editors for their generous gifts of time, energy and effort.

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SECTION-I

Electrical and Electronics Engineering

Analysis and Simulation of Uniform Step Asymmetrical Multilevel Inverter

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Abstract - This paper presents cascaded multilevel inverter(MLI) approach for high voltage and high power output applications. It is based on the series connection of the H-bridge inverter cells powered by the supplies which are in GP with different ratios like 2,3,4etc.The proposed configuration is shown for 15 level and 27 level inverters, having inherent advantages of the cascade H-bridge inverters. Structural and operational characteristics are discussed. Simulation using Matlab Simulink is done to verify the performance. Simulation result for this proposed scheme are shown in this paper .

Keywords - *Asymmetrical Multilevel Inverter, MATLAB simulink, Symmetrical step control techniques, , Total harmonic distortion(THD).*

I. INTRODUCTION

The emergence of multilevel inverters has been increased since last decade. These new types of inverters are suitable for high voltage and high power application due to their ability to synthesize waveforms with better harmonic spectrum. Numerous topologies have been introduced and widely studied for utility and drive applications. Amongst these topologies, the multilevel cascaded inverter was introduced in Static VAR compensation and drive systems.

The multilevel inverter [MLI] is a promising inverter topology for high voltage and high power applications. This inverter synthesizes several different levels of DC voltages to produce a staircase (stepped) that approaches the pure sine waveform . It has high power quality waveforms, lower voltage ratings of devices, lower harmonic distortion, lower switching frequency and switching losses, higher efficiency, reduction of dv/dt stresses. It gives the possibility of working with low speed semiconductors in comparison with the two-levels inverters. Numerous of MLI topologies and modulation techniques have been introduced and studied extensively. But most popular MLI topology is Diode Clamp, Flying Capacitor and Cascaded Multilevel Inverter (CMLI). In this paper we use a CMLI that consist of some H-Bridge inverters and with un-equal DC named as Asymmetric Cascaded Multilevel Inverter (ACMLI). It is implemented with uniform step because this inverter is more modular and simple in construction.

There are many modulation techniques to control this inverter, such as Selected Harmonics Elimination or Optimized Harmonic Stepped-Waveform (OHSW), Space Vector PWM (SVPWM) and Carrier-Based PWM (CBPWM), Symmetrical step control. A symmetrical step control is used for multilevel inverter because of its advantages of simple logic and easy implementation.

Asymmetrical Multi Level Inverter(Acmli) :

This method eliminates the excessively large number of bulky transformers required by conventional multi level inverters, the clamping diodes required by diode clamped multilevel inverters, and the flying capacitors required by flying capacitor multilevel inverters. This method consists a series connection of multiple H bridge inverters. Each H-bridge inverter has the same configuration as a typical single-phase full-bridge inverter. This method introduces the idea of using separate DC sources to produce an AC voltage waveform. Each H bridge inverter is connected to its own DC source. By cascading the output voltage of each H-bridge inverter, a stepped voltage waveform is produced. If the number of H-bridges is N, the voltage output is obtained by summing the output voltage of

bridges as shown in equation. Fig. 1 shows configuration of ACMLI of single-phase.

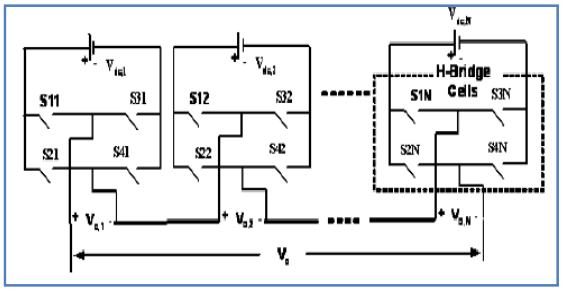

Fig. 1 : Single-phase cascaded multilevel inverter.

If ACMLI has N H-Bridges, The output voltage could be expressed as ;

$$Vo\,(t) = Vo1\,(t) + Vo2\,(t) + \ldots\ldots + Vo\,N\,(t) \qquad (1)$$

Where, $Vo1\,(t)$,$Vo2\,(t)$, ... $Vo\,N\,(t)$ are the output of individual H-bridge.

In the CMLI, the DC voltage may or may not be equal. If DC voltage given to all H-bridges is same that CMLI is called SCMLI. If DC voltage is different then it is called ACMLI.

In ACMLI DC voltage with ratio binary and ternary are the most popular. In binary progression within H-Bridge inverters , the DC voltages having ratio 1: 2: 4: 8. . : 2N and the maximum voltage output would be $(2^N\text{-}1)$ V dc and the voltage levels will be $(2^{N+1}\text{-}1)$. While in the ternary progression the amplitude of DC voltages having ratio 1: 3: 9: 27. . : 3N and the maximum output voltage reaches to $((3^N\text{- }1)/2)$ V dc and the voltage levels will be(3^N) .

II. OPERATION CHARACTERISTICS:

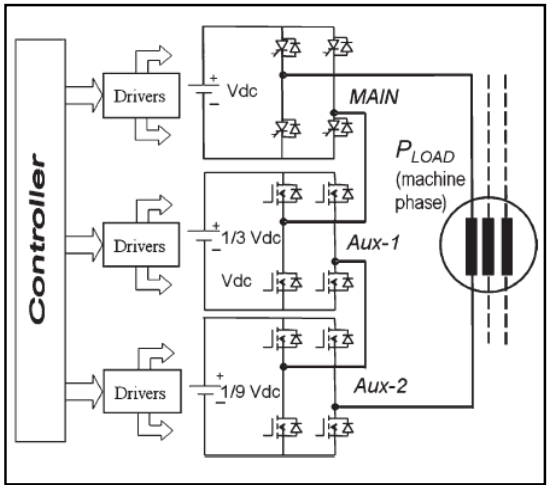

Fig. 2

One advantage of this particular Asymmetric CMLI is that most of the power delivered to the load by H Bridge having the highest DC source called "MAIN" bridge. The example of Fig. 2 shows the simulated power distribution in one phase of the 27-level MLI, as a function of output voltage. At full power, around 81% of the real power is delivered by the Main H-bridge, but only 16% from the Aux-1 bridges and approximately 3% of the total power from Aux-2 bridges.

III. SYMMETRICAL STEP CONTROL TECHNIQUE:

Among other modulation, Symmetrical step control strategies are the most popular methods used in CMLI, because they are easily implemented. Basic principle of Symmetrical step control strategies is all output steps are Symmetrical. Circuits are simulated in MATLAB/SIMULINK. For switching to the bridge switches in matlab simulink pulse generators are used. The outputs for different bridges are shown in tables.

TABLE I

VOLTAGE LEVELS OF EACH BRIDGE AND OUTPUT FOR 7 LEVEL ACMLI

Bridge 1(2v)	Bridge 2(1v)	Voltage(amplitude)
-2v	-1v	-3V
-2v	0	-2v
0	-1v	-v
0	0	O
0	1v	V
2v	0	2v
2v	1v	3v

TABLE II

VOLTAGE LEVELS OF EACH BRIDGE AND OUTPUT FOR 15 LEVEL FOR HALF CYCLE

Bridge 1(4V)	Bridge 2(2V)	Bridge 3(V)	Voltage(amplitude)
0	0	0	O
0	0	1v	V
0	2v	0	2v
0	2v	1v	3v
4v	0	0	4v
4v	0	1v	5v
4v	2v	0	6v
4v	2v	1v	7v

TABLE III

VOLTAGE LEVELS OF EACH BRIDGE AND OUTPUT FOR 9 LEVEL FOR HALF CYCLE

Bridge 1(3v)	Bridge 2(1v)	Voltage (amplitude)
0	0	O
0	1v	V
3v	-1v	2v
3v	0	3v
3v	1v	4v

TABLE IV

VOLTAGE LEVELS OF EACH BRIDGE AND OUTPUT FOR 27 LEVEL FOR HALF CYCLE

Bridge 1(9v)	Bridge 2(3v)	Bridge 3(v)	Voltage (amplitude)
0	0	0	o
0	0	1v	V
0	3v	-1v	2v
0	3v	0	3v
0	3v	1v	4v
9v	-3v	-1v	5v
9v	-3v	0	6v
9v	-3v	1v	7v
9v	0	-1v	8v
9v	0	0	9v
9v	0	1v	10v
9v	3v	-1v	11v
9v	3v	0	12v
9v	3v	1v	13v

Here TABLE I and TABLE II are having binary GP ratio for two bridges(7 level) and three bridges (15 level) respectively. Table III and Table IV are corresponding to ternary GP ratio for two bridges(9 level) and three bridges (27level) respectively. For symmetrical step control every level has duration of $\pi/8$ in 7 level inverter and for 27 level it will be $\pi/28$.

IV. SIMULATION:

For simulation of 15 level and 27 level Asymmetrical multi level inverter the model is same but the switching states and sources of power are different.

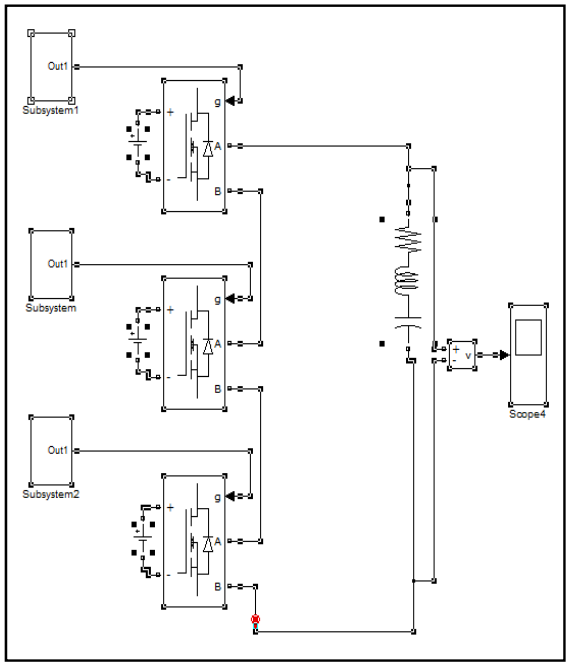

Fig. 3 : Simulink model of Asymmetrical CMLI with N=3,

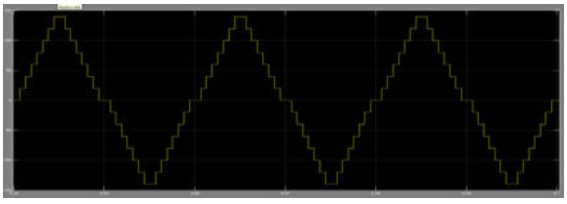

Fig. 4 : 15 level Asymmetrical Multi Level Inverter Output for ACMLI

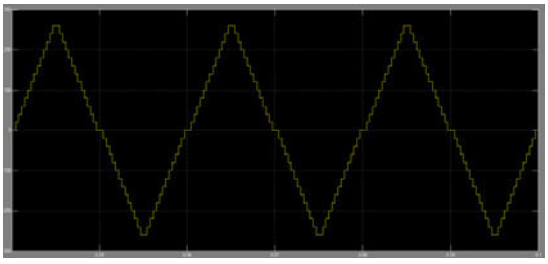

Fig. 5 : 27 level Asymmetrical Multi Level Inverter Output_ for ACMLI

V. SIMULATION RESULT AND DISCUSSION:

Results of simulations are shown in Fig.4.and Fig.5 and corresponding THD is shown in Fig.6 and Fig.7.

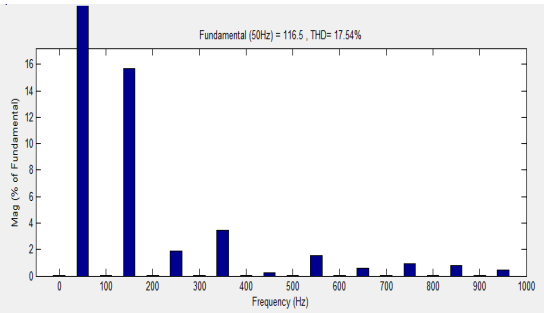

Fig. 6 : THD of 15 level inverter output

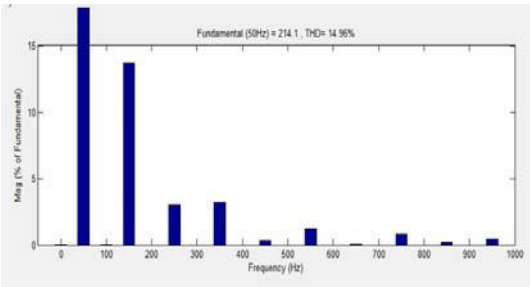

Fig. 7 : THD of 27 level inverter output

Having shown the simulation result of the 15 level and 27 level for Symmetrical step control it is observed that the Total harmonic distortion is more, hence the losses are also more in the system. But, it is the simplest method among all the methods and easy to implement in the hardware. More methods with less THD would be described in the next paper.

TABLE III

ACMLI	NO.OF BRIDGES	NO. VOLTAGE LEVELS	THD (%)
BINARY	2	7	25.47
	3	15	17.54
TERNARY	2	9	22.05
	3	27	14.96
	4	81	12.90

Above result inspires us to increase the GP ratio and the no. of bridges but it has been avoided due to following limitations.

For the same no. of bridges in ACMLI ternary GP ratio has more levels then binary GP ratio, but increasing GP ratio above ternary will not increase the voltage levels.

By using four bridges and ternary voltage ratio we can have the 81 level output voltage, but more bridges increase the cost and hence their losses, and will reduce the efficiency. Further for fourth bridge DC source is 27 times the DC source voltage for the first bridge and hence bridge requires much more different power rating still have to carry the same current. Rating of the fourth bridge would be 27 times higher than rating of the first bridge and for 81 level inverter switching losses are also increased. When we use the 3 bridges THD is 14.96 with additional one bridge it reduces to 12.9 that is not a great reduction. Hence, In ACMLI use of ternary GP ratio with three bridges that is 27 level is optimum.

VI. CONCLUSION

The scheme of Symmetrical step control technique for ACMLI was proposed to improve the output voltage of CMLI. And it has been conclude that by increasing no. of levels for the output voltage, the THD can be reduced. No. of levels can be increased by increasing the no. of bridges of MLI, Further for same no. of bridges in ACMLI, in ternary voltage progression has more voltage levels then binary and 3-bridge 27 level is an optimum value of Multi level inverter. Other methods with less THD would be considered for the future work.

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Multi-Resonating UWB Printed Monopole Antenna

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Abstract **-** Ultra wideband printed monopole antenna with multi resonating patches has been presented. The proposed antenna is designed to operate from 1.3 GHz to cover the range up to 12 GHz, which is well beyond defined ultra wideband range of 3.1 GHz to 10.6 GHz. The theoretical results have been verified with experiments with reasonably good agreement.

Keywords **-** *Multi resonating antenna; open ended resonator; ultra wide bandwidth (UWB; printed monopole antenna.*

I. INTRODUCTION

With exponential rise of wireless communication applications, and the approval of ultra wideband (UWB) for public use by the FCC in February 2002 [1], the requirement of multi-band UWB antenna has increased. Earlier, designs of single patch of square, rectangular, circular and elliptical shape printed antennae have been reported. The current distribution on these antennae is on the edges of the patch, thus antenna performance is not strongly dependent on central part of the patch. Previously, multi resonating antennae with multiple elements have been reported [2-3]. In these antennae, either size is increased or they do not fully cover the impedance bandwidth for lower end of UWB range.

The combination of two or more resonating elements will generate overlapping multiple resonances, resulting in multiband antenna or UWB antenna. When more resonating elements are present then it becomes difficult to get impedance matching for entire UWB therefore optimization is needed for feed, i.e. feed length, feed position, coupling of feed to the driver resonator and coupling between the resonators. These things have been considered for the proposed antenna to obtain UWB response. The proposed antenna in this paper has lesser effective area and hence small antenna size would be an important parameter for selection in portable communication systems [4-5]. In this paper, multi-resonator has been presented, which yields the bandwidth over 10.7 GHz centered around 6 GHz, from 1.3 GHz to 12 GHz. This range would be very useful for 1800GSM, 1900PCS, 2.4GHz Bluetooth - ISM, AWS, UWB and Radio Relay System beyond 11 GHz [4-6].

II. GEOMETRY AND DESIGN OF ANTENNA

A. Resonance frequencies

The antenna configuration is shown in Fig. 1. The multi resonating structure will have two resonances for two different elements. The outer structure is open ended resonator and will have lower edge frequency instead of resonance frequency. The f_L is approximated as given in (1) [7].

$$f_L = c/\lambda_L \qquad (1)$$

where, $\lambda_L = 2L\ [\sqrt{(\varepsilon_r + 1)/2}]$, ε_r is the dielectric constant of the FR4 substrate, which for the present case is 4.3 and the L can be measured with the help of longest current path in outer structure.

B. Geometry

The configuration is shown in fig. 1. The multi-resonating printed monopole antenna is basically using a rectangular patch of size 50 mm x 40 mm, which is designed at lower band-edge frequency of around 1.30 GHz by using equation (1) [7]. A rectangular patch of 36 mm x 37 mm has been chopped off to leave width W= 7 mm. To reduce the lower band-edge frequency, f_L, the outer structure length has been increased by 2 mm; this makes it U-fork type structure. To improve matching from source to radiator the bottom of the patch is made circular with the arc of radius = 38 mm and centre for the arc is decided by adjusting feed length of p=0.2 mm.

Second rectangular structure of size 22 mm x 29 mm is designed with the spacing S = 7 mm between two resonators. For improving of matching at the input of the second radiator, circular bottom of arc radius of 27 mm centre is optimized. The vertical gap between two radiating patches is 6.775 mm. The multi-resonating printed monopole antenna configuration is fabricated on FR4 substrate of size 50 mm x 72 mm, thickness =1.59

mm, dielectric constant, ε_r = 4.3 and loss tangent tanδ=0.01.

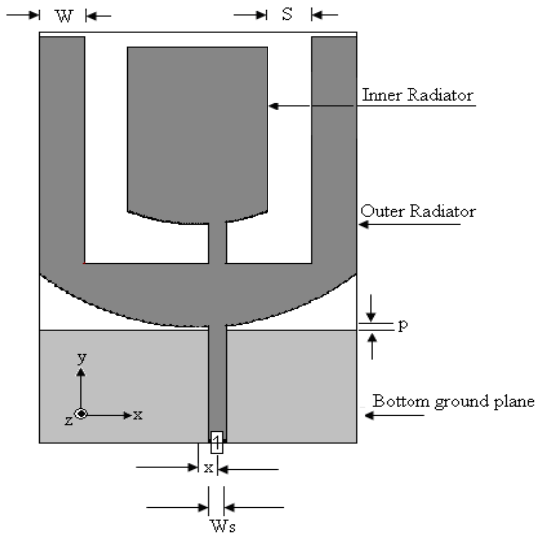


Fig. 1: Geometry of Multi-Resonating Printed Monopole Antenna

A microstrip line feed with partial backing ground plane of size 50 mm x 20 mm has been used [5], [8]. The microstrip feed line is designed with width of Ws = 2.8 mm for the impedance of 50 Ω. The feed position is optimized so that two resonators are excited with good input match, leading to larger bandwidth. The 50 Ω feed position has been chosen by moving the microstrip feed along the base (horizontally along the x-axis) of the configuration to obtain improved input match at x = 3 mm with feed length of p= 0.2 mm, as shown in Fig. 1 matching over large bandwidth is obtained [9]. The theoretical analysis of this configuration has been carried out using IE3D software [10].

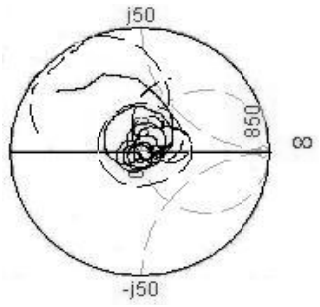
III. RESULTS

The theoretical results have been validated by experiment. The input impedance, bandwidth corresponding to VSWR ≤ 2, radiation patterns etc of this antenna have been measured. The simulated and measured input impedance loci and corresponding VSWR, are shown in Fig. 2 (a) and (b), respectively. It has been observed that the measured bandwidth for VSWR ≤ 2 is from 1.3 GHz to 12 GHz (BW = 10.7 GHz) while the corresponding simulated bandwidth is from 1.4 GHz to 11.4 GHz (BW = 10 GHz).

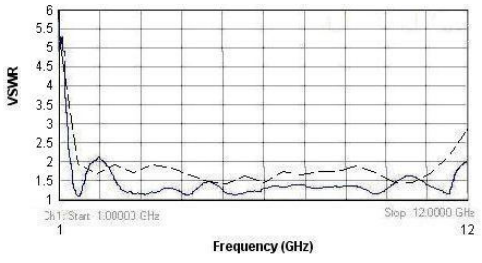
For the insight simulated current distributions of the proposed multi-resonator antenna are presented in Fig. 3. The current distribution shows the existence of resonant mode and their harmonics at higher order modes. Current distribution at 1.5 GHz shows that the outer U-fork resonates at own frequency, where as inner patch does not get excited. At 3.5 GHz inner patch resonates and outer patch gives harmonics. Similarly at 7.5 GHz and 10.5 GHz both the resonators yield higher order harmonics.

The radiation patterns were simulated over the complete impedance bandwidth and experiments were conducted to validate the same which are shown for three frequencies at 3 GHz, 6 GHz and 9 GHz. The azimuthal radiation pattern is similar to omni directional. At higher frequency, radiation patterns are similar to that of at lower frequency with more variations in radiation patterns. Fig. 4 shows the simulated and measured azumuthal radiation patterns with reasonable agreement. The differences between the measured and simulated radiation patterns are due to manual alignment errors and reflections from the various objects present inside the laboratory, where measurements were carried out.

Fig.5 shows the plots of maximum gain and radiation efficiency. The gain varies between 4 dBi to 5 dBi in the complete bandwidth and the corresponding variation in the radiation efficiency is between 98% and 92%, which makes the antenna a very efficient radiator in the required frequency range.



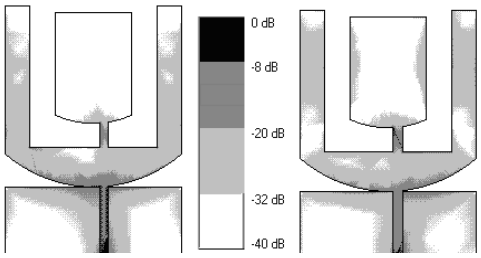
(a)



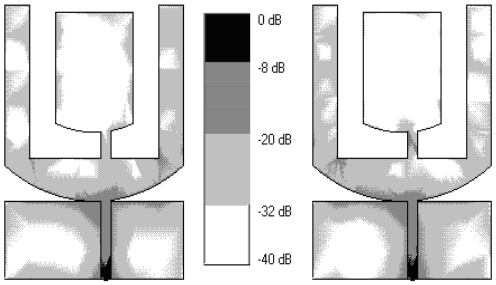
(b)

Fig. 2 : Theoretical and measured (a) Impedance Loci and (b) VSWR

(------Simulated, ____ Experimental)

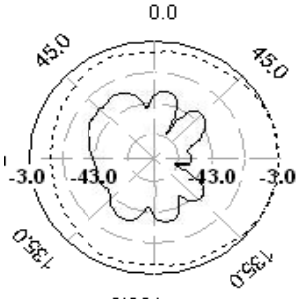


(a) 1.5 GHz (b) 3.5 GHz



(c) 7.5 GHz (d) 10.5 GHz

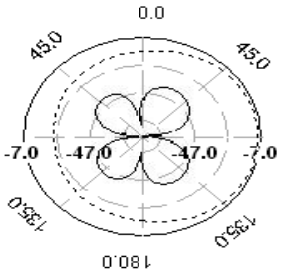
Fig. 3: Simulated current distribution at (a) 1.5 GHz (b) 3.5 GHz and (c) 7.5 GHz (d) 10.5 GHz



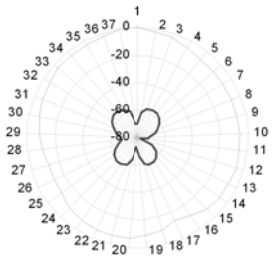
(i)

(ii)

(b) at 6 GHz

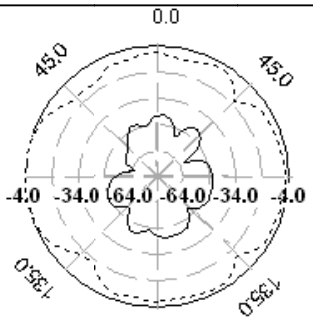


(i)

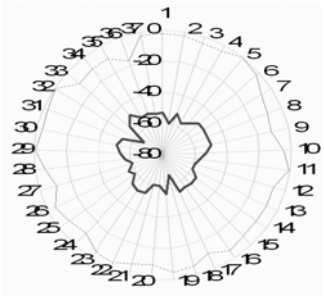


(ii)

(a) at 3 GHz



(i)



(ii)

(c) at 9.5 GHz

Fig. 4 : Simulated and measured azumuthal radiation patterns at (a) 3 GHz (b) 6 GHz and (c) 9.5 GHz (i) Simulated, (ii) Experimental (------Co-pol, ——— Cross-pol)

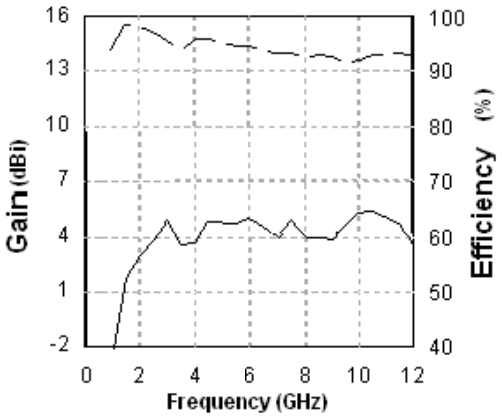


Fig. 5 : Maximum gain and radiation efficiency versus frequency (GHz) (----efficiency, ——— gain)

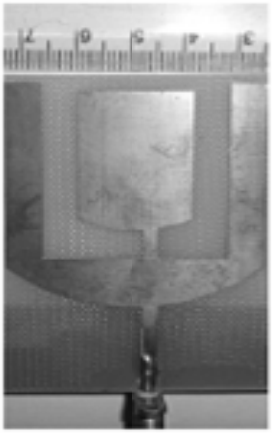


Fig. 6: Photograph of the fabricated Multi-Resonating Printed Monopole Antenna

Fig. 6 shows the photograph of the fabricated antenna of optimized configuration.

IV. CONCLUSION

A very simple design of multi-resonating UWB antenna has been proposed. The proposed printed monopole antenna has radiation pattern similar to the conventional dipole antenna. The antenna yields ultra wide bandwidth. The measured and simulated bandwidth ratio of this antenna is 10.7:1 and 10:1, respectively for VSWR $\leq$ 2:1, which is very useful range for many communication bands.

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Performance Evaluation of Multiplier - Architecture Based on Switching Activity Minimization

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Abstract - Multipliers are the fundamental components of many digital systems. It has wide range of applications in digital signal processing, wireless sensor networks and portable digital systems and hence their power and area are of prime concern. Power management has become a great concern in VLSI design in recent years. Power consumption in conventional multiplier mainly depends on switching activities and hence leads to more power dissipation. In this paper modifications are done in shift and add architecture of multiplier by removal of shifting in B register, direct feeding of A to the adder, bypassing the adder whenever possible, using a ring counter instead of a binary counter and removal of the partial product shift for minimizing the switching activity, thereby reducing the power consumption and area occupied. The simulation results shows that shift and add architecture occupies only 50% of area and saves power five times compared to conventional multiplier.

Keywords - *Low-power multiplier, Low-power ring counter, Shift-and-Add multiplier, switching activity reduction.*

I. INTRODUCTION

Research in VLSI towards reduction in area, power, cost and increase in performance and reliability of the circuit. However, this has begun to change and, increasingly, power is being given comparable weight to area and speed considerations. The wireless communications systems such as personal digital assistants, personal communicators, portable desktops, audio- and video-based multimedia products needs high-speed computation and low power consumption. To save significant power consumption of a VLSI design, it is a good direction to reduce its dynamic power that is the major part of total power dissipation.

The power consumption in digital CMOS circuit can be described by the following expression:

$$\mathbf{P_{avg} = P_{Dynamic} + P_{Shortcircuit} + P_{Leakage} + P_{Static}}$$

The dynamic power dissipation is caused by charging and discharging of capacitances in the circuit. The short circuit power consumption is caused by the current flow through the direct path existing between the power supply and the ground during the transition phase. The n-MOS and p-MOS transistors used in a CMOS logic circuit commonly have non zero reverse leakage and sub threshold current.

Multipliers are fundamental components of digital hardware. They occupy a relatively large portion of the overall chip area and have often been the limiting factor in terms of speed. The computation of a multiplier manipulates two input data to generate many partial products for subsequent addition operations, which in the CMOS circuit design require many switching activities. Switching activity of a circuit can be expressed as the summation over all operation types performed, as the product of operation frequency and the number of transitions per operation. The switching activities within the functional unit of a multiplier accounts for the majority of the power dissipation of a multiplier, as given in the following equation:

$$\mathbf{P_{Switching} = \alpha\ c\ v_{dd}^2\ f_{clk}}$$

Where $\boldsymbol{\alpha}$ is the switching activity parameter, $\mathbf{c}$ is the loading capacitance, $\mathbf{v_{dd}}$ is the operating voltage and $\mathbf{f_{clk}}$ is the operating frequency. Minimizing the switching activities can effectively lower power dissipation without affecting the circuit operation performance.

The generation of partial product and shifts in registers leads to more consumption of power and area. Among multipliers, the carry-select-adder based radix multipliers, which have lower area overhead, employ a greater number of active transistors for the

multiplication operation and hence consume more power. The tree multipliers are used in high speed applications such as filters, but these require large area. Higher-radix multipliers are faster but consume more power since they employ wider registers, and require more silicon area due to their more complex logic. Among other multipliers, shift-and-add multipliers have been used in many other applications for their simplicity and relatively small area requirement [1]-[3]. In this paper, the shift and add architecture is designed and it has more power advantage compared to other multipliers.

This paper is organized as follows: Section II briefly reviews the background information about conventional shift and adds multiplier. Section III describes the architecture description of the low power multiplier. Section IV describes the low power ring counter architecture. Results are discussed in section V and conclusion is in the last section.

II. SHIFT AND ADD MULTIPLIER

The architecture of a conventional shift-and-add multiplier, which multiplies A by B, is shown in Figure 1. The dashed ovals show the major sources of switching activities. The multiplier is shifted in each cycle and the bit which getting out of register B is connected to the select pin of multiplexer, mux_A. As the select signal changes, the output of mux_A also changes. This causes the adder operation. The partial product is required to be shifted in every cycle. The counter is for checking whether the required number of operations has been performed. The six major sources of switching activity are: (a) Shifting of the 'B' register. (b) Activity in the counter. (c) Activity in the adder. (d) Switching between '0' and 'A' in the multiplexer. (e) Activity in the multiplexer select. (f) Shifting of the partial product register. By eliminating or reducing the switching activity described above, low power architecture can be derived.

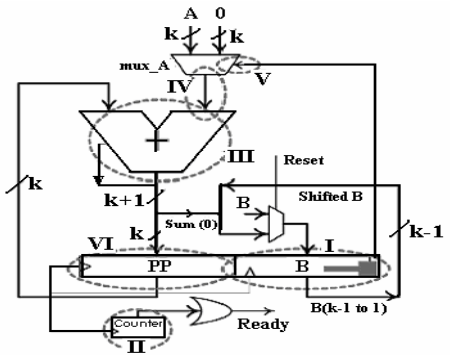

Fig. 1 : Architecture of conventional Shift and Add multiplier with major source of switching activity

A. B REGISTER:

To generate the partial product, B (n) is used to decide between A and 0. If the bit is "1", A should be added to the previous partial product, whereas if it is "0", no addition operation is needed to generate the partial product. Hence, in each cycle, register should be shifted to the right so that its right bit appears at B (n) this operation gives rise to some switching activity.

B. ADDER:

In each cycle, the current partial product is added to A (when B (n) is 1) or to 0 (when B (n) is 0). This leads to unnecessary transitions in the adder when B (n) is zero.

C. PARTIAL PRODUCT REGISTER:

In each cycle, the current partial product is added to A (when B (n) is 1) or to 0 (when B (n) is 0). This leads to unnecessary transitions in the adder when B (n) is 0; the partial product is shifted in each cycle giving rise to transitions. The multiplication algorithm reveals that multiplication may be completed by processing the most significant bits of the partial product and hence, it is not necessary for the least significant bits of the partial product to be shifted. The data transparency problem of latches prohibits us from using latches instead of flip-flops for forming the lower half of the partial product.

III. LOW POWER MULTIPLIER

The architecture of a low power multiplier is shown in Figure 2. The major modifications made are the removal of the multiplier shifting, direct feeding of multiplicand to the adder, Reduction in partial product shifting, bypassing the adder whenever possible and use of a ring counter instead of a binary counter.

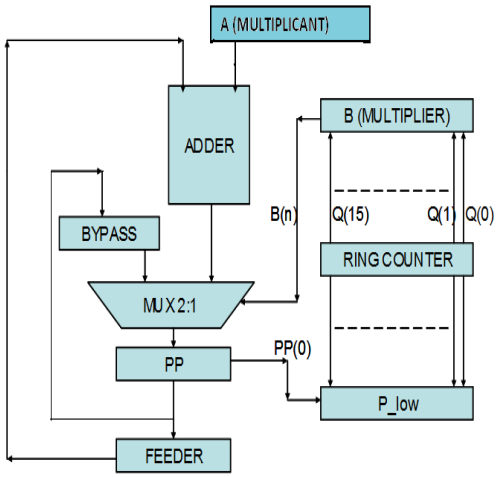

Fig. 2 : Architecture of Low Power Multiplier

A. SHIFTS OF B-REGISTER

To generate partial product in conventional architecture B (0) is used to decide between A and 0. In each cycle, register B should be shifted to right giving rise to more switching activity. The shift and add multiplier is proposed where the multiplexer with one hot encoded bus selector chooses the hot bit of B in each cycle. A Ring counter is used to select B (n) in nth cycle thereby reducing the switching activity.

B. ACTIVITY OF ADDER

There is an unnecessary transition in adder when B (n) is 0 in conventional multiplier. In such cases, the adder can be bypassed and the partial product should be shifted to right by one bit. So, in Shift and Add Multiplier the feeder and bypass registers are used to bypass the adder in the cycles when B (n) is 0. In each cycle, the hot bit of the next cycle is checked. If it is 0, the adder is not needed in the next cycle; the bypass register is clocked to store the current partial product. If it is 1, the adder is really needed in the next cycle; the feeder register is clocked to store the current partial product which must be fed to the adder in the next cycle. To select between the feeder and the bypass registers NAND and NOR gates of inverting logic is used. When the hot bit B (n) is 0, there is no transition in the adder. This enables to remove the multiplexer and feed input A directly to the adder, reducing in a noticeable power saving.

C. *SHIFTS OF PARTIAL PRODUCT REGISTER*

In the conventional architecture, the partial product is shifted in each cycle giving rise to transitions. The multiplication algorithm reveals that the multiplication may be completed by processing the most significant bits of the partial product. It is not necessary for the least significant bits of the partial product to be shifted. In the Shift and Add architecture, for lower half of partial product we use latches. So, the least significant bit (LSB) of PP (0) is stored in right most latch of PP register. The ring counter output is used to open the proper latch when he last bit is stored in the left most latch, the higher and lower halves of the PP form the final product result.

Power is saved by two reasons,

1) Lower half of the PP is not shifted.
2) This half is implemented with latches instead of Flip flops.

IV. RING COUNTER

The counter used in the conventional multiplier has large number of switching activities. An n bit synchronous ring counter is built by cascading n flip flops in a chain. The conventional Ring Counter is shown in the figure 3.

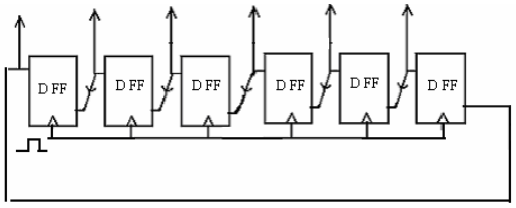

Fig. 3 : Conventional synchronous ring counter

All flip flops have a common clock signal and each clock pulse is applied to all flip flops whereas the movement of '1' in the counter chain reveals that each clock pulse must be applied to only two flip flops. So, in each clock pulse (n-2) x s unnecessary transitions are raised where, 's' is the total number of transitions raised in single flip flop, 'n' is the number of flip flops.

A. *SHIFTING OF THE MULTIPLIER USING RING COUNTER*

An example of a shift and add Multiplication is

```
A →      011   X
B →      010   =
         ----------
          0 0 0          (B (0) = 0)
        0 1 1            (B (1) = 1)
      0 0 0              (B (2) = 0)
     ----------------------
     Answer →  0 0 1 1 0
```

Fig. 4 : Shift and Add Multiplication

In each step for generating the partial product, the corresponding bit of the multiplier is needed; it is shown as B (0), B (1) and B (2) in figure 4. For getting the corresponding multiplier bit, the multiplier is required to be shifted. If the required bit is obtained without shifting, considerable power saving can be achieved. This is achieved by using a ring counter as shown in Figure 5.

B. *LOW POWER RING COUNTER*

The ring counter used in the shift and add multiplier is noticeably wider than the binary counter used in the conventional architecture. To minimize the switching activity of the counter we use low power ring counter.To reduce the switching activities only some flip flops can be clock gated. A flip flop in a ring counter must be clocked if and only if either its input or output is '1' immediately before the triggering clock edge comes. So only two flip flops must be clocked in each cycle.

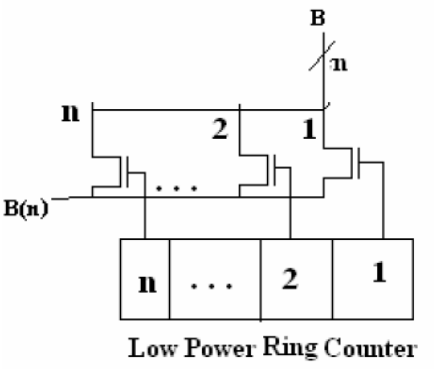

Fig. 5 : Low Power Ring Counter

The clock gating logic with flip-flops' input and output is shown in the figure 6,OR's the value of flip flop's input and output on Positive clock edges stores the result in latch. The output of the latch determines whether or not to gate the clock signal .This clock gator is positive edge triggered.

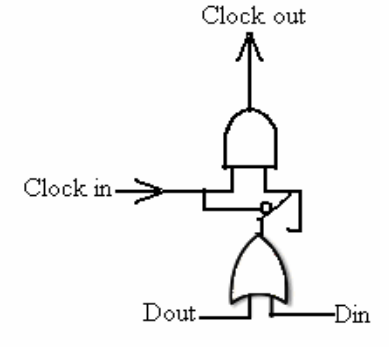

Fig. 6 : Clock Gating Structure

To avoid all the unnecessary transitions raised by the clock signal each flip-flop should be provided with the clock gating circuitry of above figure 6, but this solution ends up with a large area overhead plus due to transitions in clock gator themselves the resulting ring counter will not have fewer switching activity. A better solution is used in the low power multiplier architecture.

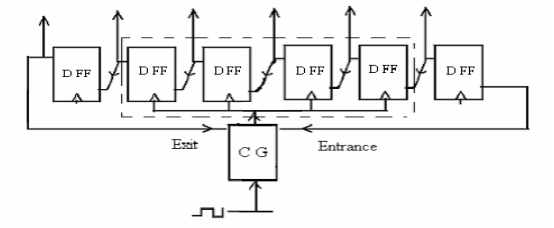

Fig. 7 : Low Power Architecture for Ring Counter with Block of Size 4

One of the important properties of the ring counter is that its output is one hot encoded. This property of the ring counter makes its output wide especially as the counter size increases. To reduce the switching activity of the counter the counter is partitioned in to a number of blocks which are clock gated with a special clock gating structure whose power and area overheads are independent of the block size, controlling with the low power ring counter helps to get a low power low area architecture, thus avoids the trade off between power and area [5], [8], [9]. The clock gating structure is shown below Fig 8.

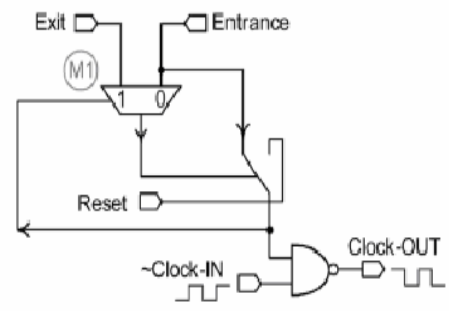

Fig. 8 : Clock Gating Structure for the Low Power Ring Counter

The clock gating structure for hot block ring counter is composed of a multiplexer, a NAND gate, and a resettable latch. In addition to the reset and clock IN signals, there are two other signals called Entrance and Exit, coming from the neighboring left and right blocks. These are used to determine whether the '1' is present in the block to which the output of the Clock gating goes.

V. RESULTS AND DISCUSSIONS

Low Power Shift and Add Multiplier of 8 bit is verified using MODELSIM10.0a with VERILOG code. The comparison of multipliers in terms of Power and Area is shown in Table 1.

Table 1: Simulation results for 8-bit multipliers

PARAMETERS	CONVENTIONAL MULTIPLIER	SHIFT AND ADD MULTIPLIER
POWER (mW)	1244	253.65
AREA (slices)	180	96

The graphical representation of multipliers in terms of Power and Area is shown in figure 9 and figure 10.

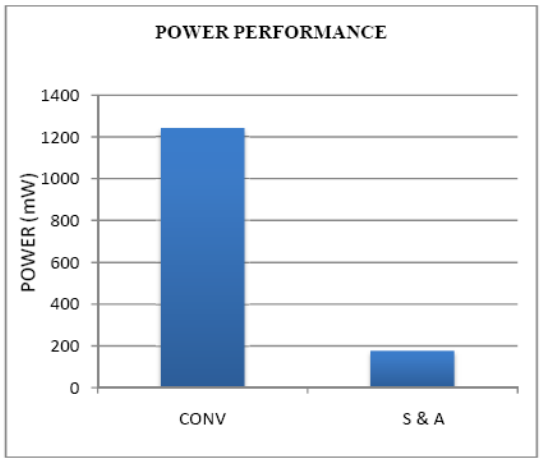

Fig. 9 : Comparison between Conventional Multiplier with Low Power Multiplier in terms of Power

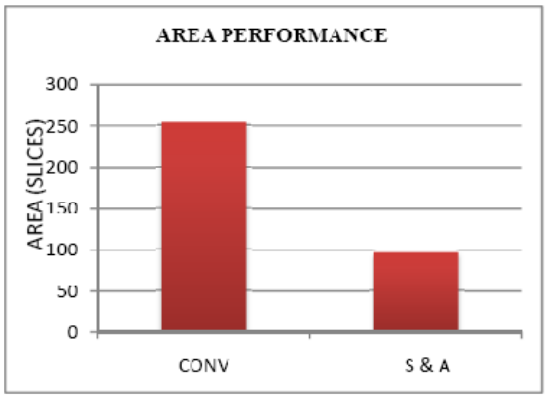

Fig. 10 : Comparison between Conventional Multiplier with Low Power Multiplier in terms of Area

When compared to conventional multiplier, the shift and add architecture occupies 50% of area and hence area minimization occurs. Also power consumption is five times lower than conventional multiplier.

VI. CONCLUSION

The multiplier is explored based on shift and add architecture. The multiplier system is suitable mainly for portable digital systems, microelectronic devices, DSP's. The modifications to the conventional architecture included the removal of the shift of the B register, direct feeding of A to the adder, bypassing the adder whenever possible, use of a low power ring counter instead of the binary counter, and removal of the partial product shift. Low-power architecture for ring counters is proposed based on partitioning the counter into blocks of flip-flops clock gated with a special clock gating structure and the complexity of which was independent of the block sizes. The simulation results prove that shift and add multiplier performance is better than conventional multiplier. Therefore, this multiplier is feasible for any low power low area applications.

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Efficient Bit-Parallel Systolic Multiplier for Special Class of GF (2^m)

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Abstract **-** A bit parallel systolic multiplier in the finite field GF(2^m) over the polynomial basis where irreducible polynomial, all one polynomial (AOP) and an irreducible trinomials generate the field GF(2^m) is presented. The complexity of the multiplier is compared in terms of area, latency and power. The AOP based multiplier and the multiplier with irreducible trinomial has high throughput as compared with the traditional systolic multipliers. Moreover, these multipliers are highly regular, modular, and therefore, well-suited for VLSI implementation.

Keywords **-** *Galois Field, cryptography, Bit parallel systolic multiplier, AOP.*

I. INTRODUCTION

Finite fields of the form GF(2^m) have found applications in the implementation of error-correcting codes such as Reed-Solomon (RS) codes and also certain cryptographic systems [1-3]. Addition and multiplication are two basic arithmetic operations in finite fields. Addition operation is easily realized using XOR gates but the multiplication operation is costly in terms of component counts and time delays [4]. Finite field multiplication is the most important arithmetic operation because it is nontrivial to implement in hardware and frequently required in both the encoding and decoding algorithm of cryptography. The other operations such as division and exponentiation can be performed by repeated multiplication. This study focuses on the hardware implementation of fast and low-complexity multipliers over GF(2^m) since computing exponentiation, division, and computing multiplicative inverse can be performed by computing multiplication iteratively. Many bit parallel systolic multipliers have been proposed in [5-7], the fields in these multipliers are defined by irreducible polynomial. However, they are inefficient for cryptographic applications due to the system's complexity. In this paper, general polynomial, irreducible trinomial systolic multiplier over GF(2^m) and AOP based simple bit parallel systolic architecture, using redundant basis are compared. The first multiplier is composed of m^2 identical cells. Each cell consisting of two 2-input AND gate and two 2-input XOR gate. The second multiplier circuit includes m^2 'U' cells and (m-1) 'V' cells, in which the 'U' cell is composed of one 2- input AND gate, one 2- input XOR gate and 'V' cell consists of one 2- input XOR gate. The third one is composed of $(m+1)^2$ identical cells, each consisting of one 2-input AND gate and one 2-input XOR gate. The latency of the systolic multiplier using irreducible trinomial is only (2m-1) clock cycles with a throughput rate of one result per clock cycle. The clock period is given by the propagation delay of a signal through a 2-input AND gate and 2- input XOR gate.

II. PRELIMINARIES

Galois field (GF) is a popular name for a field with finite number of elements. The simplest example of a GF is the binary field which consist of elements {0, 1} and referred to as GF(2). We can create larger fields by extending GF(2) into vector space leading to finite fields of size 2^m. These are simple extensions of the base field GF(2) over 'm' dimensions. Field element can be derived by two alternate representations. In the first representation, all elements of GF(2^m) may be represented as powers of a primitive field element α[2], for example if m=8,then the field element is of the form α^n for n=0,1,....255. In the second representation, each element has an equivalent representation as a binary m-bit. A polynomial of the form P(x) = $(p_0 + p_1x + p_2x^2 + \cdots + p_mx^m)$ over GF (2) is called an all in one polynomial of degree 'm'. For an irreducible polynomial of degree 'm', the polynomial P(x) is formed as $x^m + x^n + 1$ with $m > n > 0$ is known as a trinomial polynomial.

Galois field includes three different basis namely polynomial (standard), normal and dual basis. The polynomial basis of GF(2^m) can be expressed in the form $\{1,\alpha,\alpha^2,.....\alpha^{m-1}\}$, where 'α' ∈ GF($2^m$) be the root of a primitive polynomial of degree 'm' over GF(2). The primitive polynomial p(x) can be written as $(1+x^2+x^3)$ for the finite field over GF(2^3). When using a polynomial basis representation, any element of the field GF(2^m) can be expressed as a binary polynomial of degree at most (m-1). The standard alternative basis for polynomial basis is a normal basis which is represented in the form $\{\alpha, \alpha^2, \alpha^4,..... \alpha^{(2)\hat{}m-1}\}$ where 'α' is the root of an primitive polynomial of degree 'm' over GF(2). A dual basis is not a concrete basis like the polynomial basis and the normal basis rather it provides a way of using a second basis for computations. Consider two bases for elements in a finite field GF(2^m) such that $B_1 = \{\alpha_0,\alpha_1,\alpha_{2,.....}\alpha_{m-1}\}$ and $B_2=\{\gamma_0,\gamma_1,\gamma_{2,}.....\gamma_{m-1}\}$ then B_2 can be considered a dual basis of B_1 provided that Tr $(\alpha_i . \gamma_j) = \{0$, if i ≠ j and 1, otherwise. 'Tr' denotes the trace function in dual basis. This basis provides a way to easily communicate between devices that use different bases, rather converting explicitly between the bases using the change of bases formula.

Normal basis representation offers the best performance in hardware [8-10] and polynomial basis representation is more efficient in software. Using the normal basis representation, the squaring of an element in GF(2^m) is readily shown to be a simple cyclic shift of its binary digits. The main difficulties for fast normal basis multiplication in software are due to the particular computation process. First, when multiplying two elements represented in normal basis according to the standard formula, the coefficients of their product need to be computed one bit at a time. Second, the computation of a given bit involves a series of "partial sums" which need to be computed sequentially in software. To avoid the above difficulties, the normal basis multiplier realized in hardware which performs the two computations in parallel [11]. Polynomial basis multipliers are more efficient and most widely used when compared with multipliers based on normal or dual basis because polynomial basis multiplication requires a polynomial multiplication followed by a modular reduction. In practice, these two steps can be combined.

Mastrovito [12] developed a new method for multiplication where a product matrix was introduced to combine the above two steps together. The dual basis multiplier uses the dual basis representation for the multiplicand and standard basis for the multiplier. The product is again in dual basis representation and this kind of multiplier can be used in RS encoding and decoding circuits and since dual basis multiplier have particularly low hardware requirements. The multipliers over GF(2^m) may be either systolic or non systolic. In multiplier implementations, many architectures applied systolic array concept. In general, a non systolic architecture has global signals. Hence if 'm' becomes large, propagation delay also increases. But the systolic architecture does not suffer from those problem because the systolic architecture consists of replicated basic cells and each basic cell is connected with its neighbouring cells through pipelining, i.e., there are no global signals. Consequently, the systolic architecture is a better choice than the non systolic architecture for a high-speed VLSI implementation. Various architectures for non-systolic style have already been presented in [12]. The various algorithms and hardware architectures for systolic multipliers over GF(2^m) have proven their efficiencies. These techniques provide optimal design of multipliers over GF(2^m) with respect to complexities, delay and power. Most techniques focused on VLSI implementation and synthesis of these multipliers because VLSI implementations of these circuits are very complicated due to complex routing, non-modularity and low testability.

III. BIT PARALLEL SYSTOLIC MULTIPLIER

3.1 Multiplication with irreducible polynomial:

Let A (x) and B (x) be the two elements in GF(2^m), P(x) be the primitive polynomial used to generate the field GF(2^m) and C (x) be the result of multiplication where C (x) =A (x) . B (x) mod P(x). Then A (x), B (x), P (x) and C (x) can be expressed as follows:

$$A(x) = a_{m-1}x^{m-1} + a_{m-2}x^{m-2} +.....+ a_1x + a_0$$

$$B(x) = b_{m-1}x^{m-1} + b_{m-2}x^{m-2} +.....+ b_1x + b_0$$

$$P(x) = x^m + p_{m-1}x^{m-1} +.....+ p_1x + p_0$$

$$C(x) = c_{m-1}x^{m-1} + c_{m-2}x^{m-2} +.....+ c_1x + c_0$$

The LSB-first multiplication can be performed as follows:

$$C(x) = A(x) . B(x) \bmod P(x)$$
$$= b_0A(x) + b_1[A(x).x \bmod P(x)] +$$
$$b_2[A(x).x^2 \bmod P(x)] +.....+$$
$$b_{m-1}[A(x).x^{m-1} \bmod P(x)].$$

In the LSB-first scheme illustrated in [7], the multiplication starts with the LSB of the multiplier B (x) and each cell in the i^{th} step where $(1 \le i \le m)$, performs the following computations. Multiplication over GF(2^m) is associative.

$$A(x)^{(i)} = [A(x)^{(i-1)}] . x \bmod P(x)$$

$$C(x)^{(i)} = A(x)^{(i-1)}b_{i-1}+C(x)^{(i-1)}$$

Where C $(x)^{(0)} = 0$ and A $(x)^{(0)}$ = A (x)

LSB-first multiplication algorithm

Input: P (x),A (x) and B (x)

Output: C (x) = A (x).B (x) mod P (x)

Initialize: A $(x)^{(0)}$ *= A (x), C* $(x)^{(0)}$ *= 0*

For i = 1 to m do

For k = m-1 down to 0 do

$$a_k^{(i)} = a_{k-1}^{(i-1)} + a_{m-1}^{(i-1)} p_k$$

$$c_k^{(i)} = a_k^{(i-1)} b_{i-1} + c_k^{(i-1)}$$

End for

End for

C (x) = $C^{(m)}$ *(x)*

In the above algorithm $a_k^{(i)}$ and $c_k^{(i)}$ denote the k^{th} coefficient in $A^{(i)}$ (x) and $C^{(i)}$ (x) respectively and b_i denotes i^{th} coefficient of B (x) and p_k denotes k^{th} coefficient of P (x). Based on the algorithm, the signal flow graph (SFG) for 'm' is drawn as shown in the figure 1 where 'm' denotes the size of the multiplier. From the SFG, it is shown that the (m x m) cells are required to implement the multiplication over GF(2^m).The SFG is used for calculating the partial product and final output. The basic cell consists of two AND gates and two XOR gates. The internal architecture of the $(i,k)^{th}$ cell is given in figure 2. Note that in SFG, the right most cell in the first receives the input a_d which is given from the output of the previous cell but there is no previous, hence the value of a_d for all the cell in the right most column is zero.

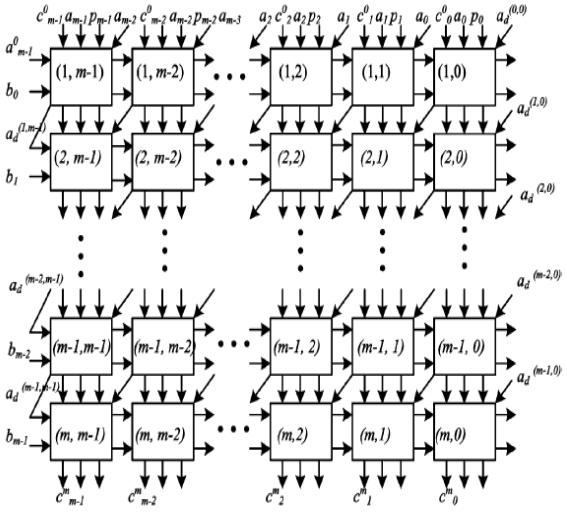

Fig. 1: SFG for multiplication over GF(2^m)

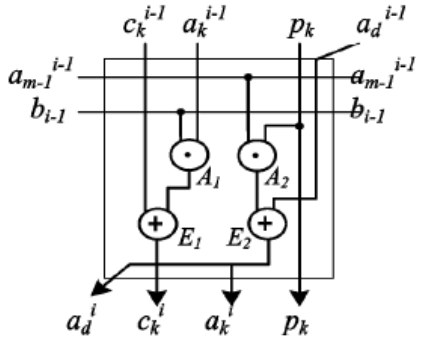

Fig. 2 : Circuit of $(i,k)^{th}$ cell

The polynomial input and polynomial output in a cell is same since it is used only for computation. Each cell computes $a_k^{(i)}$ and $c_k^{(i)}$ which is the coefficient A $(x)^{(i)}$ and C $(x)^{(i)}$. The results of the basic cells in a row are given to the next row. The final result is obtained from the last row. Note that in LSB-first algorithm, the basic cell includes multiplying by x, current partial-product generation, and accumulation-to-previous-result. These operations are performed concurrently in the LSB-first scheme, but sequentially in the MSB-first scheme. This multiplier requires m^2 identical cells and initial delay of '3m' clock cycles.

3.2 Multiplication with redundant basis:

In extended basis the multiplication of A(x) by x can be performed by shifting A cyclically once to the right [13]. That is, let A (x) = $(a_0 + a_1x + ...+a_{m-1}x^{m-1} + a_mx^m)$ then x.A(x) = $(a_m + a_0x + a_1x^2 + ...+a_{m-1}x^m)$, note that $x^{m+1} = 1$ in the extended basis. For an AOP primitive polynomial, the multiplication in extended basis can be performed as follows. Consider two elements, A and B of the extended basis. Let α be a root of the irreducible AOP. Then the product P = A.B = $(a_0 + a_1x + ...+a_{m-1}x^{m-1} + a_mx^m)$. $(b_0 + b_1x + ...+b_{m-1}x^{m-1} + b_mx^m)$. The product of the multiplication can be simplified as shown below.

$$P = \sum_{i=0}^{m} \sum_{j=0}^{m} A_{(i-j)} B_j \alpha^i$$

The simplified formulation and architecture for the bit parallel systolic multiplier based on the redundant basis for AOP of degree 'm' can be performed using the Toeplitz matrix manipulation. A Toeplitz matrix or diagonal-constant matrix is a matrix in which each descending diagonal from left to right is constant. For instance, the following {m x m} matrix D is a Toeplitz matrix [15]. If the $(i,j)^{th}$ element of D is denoted by $d_{i,j}$ then we have $d_{i,j} = d_{i-1,j-1}$.

$$D = \begin{matrix} d_0 & d_{-1} & d_{-2} & \dots & \dots & d_{-m+1} \\ d_1 & d_0 & d_{-1} & \dots & \dots & \dots \\ d_2 & d_1 & \dots & \dots & \dots & \dots \\ \dots & \dots & \dots & \dots & d_{-1} & d_{-2} \\ \dots & \dots & \dots & d_1 & d_0 & d_{-1} \\ d_{m-1} & \dots & \dots & d_2 & d_1 & d_0 \end{matrix}$$

Then we can define the (m+1) x (m+1) Toeplitz matrix and the multiplication of two elements A(x) and B(x) can be expressed in the following matrix. A systolic signal flow graph (SFG) and the internal architecture of basic cell for the AOP multiplier based on the algorithm presented in Fig 3 are given in Figure 4and 5, respectively. The elements i and j represent a row and a column of the SFG.

$$\begin{pmatrix} p_0 \\ p_1 \\ p_2 \\ . \\ . \\ P_m \end{pmatrix} = \begin{pmatrix} b_0 & b_m & b_{m-1} & \dots & \dots & b_1 \\ b_1 & b_0 & b_m & \dots & \dots & . \\ b_2 & b_1 & \dots & \dots & \dots & . \\ . & \dots & \dots & \dots & b_m & b_{m-1} \\ . & \dots & \dots & b_1 & b_0 & b_m \\ b_m & \dots & \dots & b_2 & b_1 & b_0 \end{pmatrix} \begin{pmatrix} a_0 \\ a_1 \\ a_2 \\ . \\ . \\ a_m \end{pmatrix} \quad \text{---}$$

Input: A (x), B (x) and m.

Output: P (x) = A (x).B (x) mod g (x)

Initialize: for (j = 0; j <= m; j = j+1),p (0,j) = 0;

A = [a_m, a_{m-1}, ... a_1, a_0], B = [b_m, b_{m-1}, ... b_1, b_0]

1. for i in 1 to (m+1) do

2. for j in 0 to m do

3. p (i,j) = p(i-1,j) + a(i-1).b(j)

4. end for

5. Circular right shift one bit position of B

6. end for

Fig. 3 : Algorithm

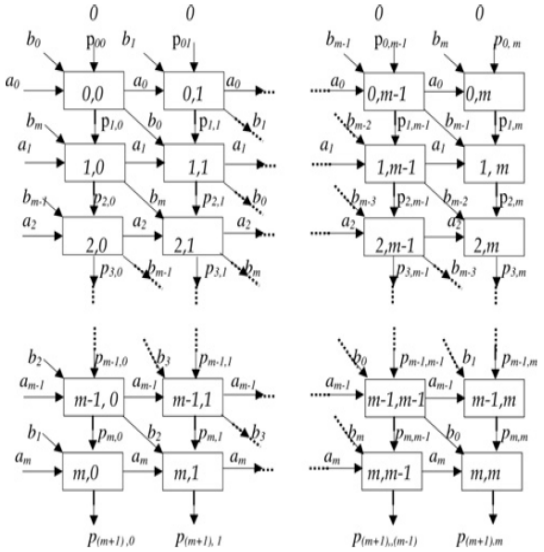

Fig. 4 : Systolic SFG for multiplication in GF (2^m)

In general, the SFG consists of (m + 1) × (m + 1) basic cells for multiplication over GF(2^m). The basic cell in the i^{th} row and j^{th} column computes p(i+1, j)th internal product in (Fig. 4). The final product P(x) in vector form is given by an array of p(m + 1, j)s. To implement the SFG as a bit parallel multiplier, the outputs of the basic cells shown in fig 5 can be latched using a D flip-flop. This implementation consumes (m + 1)^2 two-input

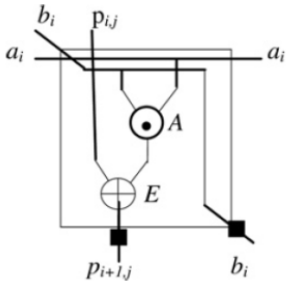

Fig. 5: Basic cell

XOR gates, (m + 1)^2 two-input AND gates and 2m^2 D-flip-flops. The primary inputs of the SFG are assumed to be not latched. This requires 'm' clock cycles to calculate one product.

3.3 Multiplication with irreducible trinomial:

This Section presents parallel systolic multiplier over the field GF(2^m) in which an irreducible trinomial of degree 'm' generates the finite field GF(2^m) discussed in [14]. For simplicity, the finite field GF(2^4) is used as an example to illustrate the architecture. Assume that

$P(x) = x^4 + x^3 + 1$ is used in the generation of the systolic multiplier. Let

$A(x) = a_0 + a_1x + a_2x^2 + a_3x^3$ $B(x) = b_0 + b_1x + b_2x^2 + b_3x^3$. The product $C(x) = A(x)\,B(x) \bmod P(x)$ can be computed as the following iterative form:

$$T_i = T_{i-1}x + B(x)\, a_{m-1} \bmod P(x)$$

$$T_0 = 0$$

$$T_m = C(x)$$

Where $T_i = t_{0,i} + t_{1,i} + t_{2,i} + t_{3,i}$ over $GF(2^m)$ represent the i^{th} intermediate product of A(x) and B(x). The above computing procedure can be realised by a parallel-in parallel-out systolic array, as shown in figure 8, where 16 basic 'U' cells and 3 basic 'V' cells are used. Each U cell at position (i,j) is denoted by $U_{i,j}$ performs the following operation, as depicted in figure 6.

$$t_{i,j} = t_{i-1,j} + a_i\, b_{(n+i-j)}$$

Each V cell at position V_i performes the following logic operation, as shown in figure 7.

$$b_{(n-i)+m} = b_{(m-i)+m}\, b_{(n-i)}$$

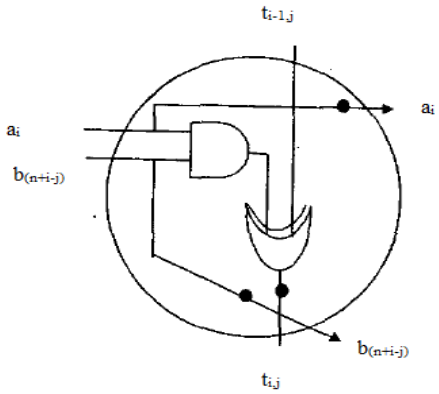

Fig. 6 : The detailed circuit of $U_{i,j}$ cell

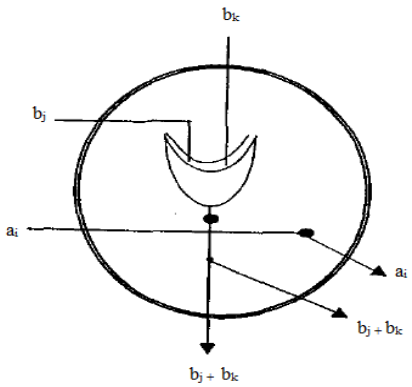

Fig. 7 : The detailed circuit of V cell

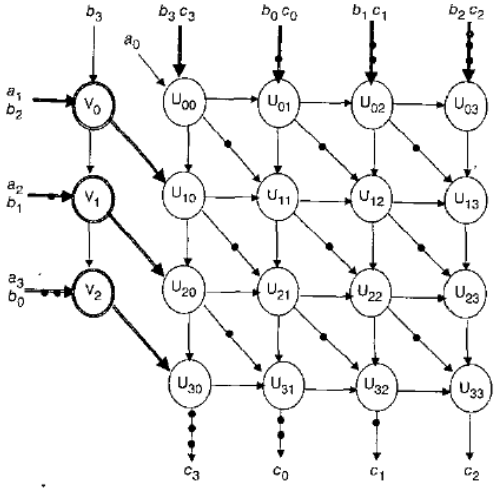

Fig. 8 : Bit-parallel systolic multiplier over $GF(2^m)$ generated by $x^4 + x^3 + 1$

IV. COMPARISON AND DISCUSSION

The bit parallel systolic multiplier over $GF(2^m)$ for irreducible polynomial, trinomial and AOP have been presented. The architecture of the irreducible polynomial multiplier can also be adopted to implement AOP based multipliers and irreducible trinomial based multiplier, by reducing the complexity of basic cell and ultimately the overall system complexity can be reduced. We therefore compare the parallel multiplier of a general $GF(2^m)$, AOP multiplier and multiplier over irreducible trinomial.

Table I reveals that the multiplier with irreducible trinomial has a smaller hardware complexity and a smaller latency than the traditional general polynomial multiplier. In addition, the trinomial multiplier has the same cell complexity. The latency of AOP based multiplier is shorter than parallel-in parallel-out systolic multiplier of $GF(2^m)$ over irreducible polynomial and trinomial. Unfortunately, irreducible AOP's are very rare. For $m \leq 100$, the values of 'm' for which an AOP of degree 'm' is irreducible are (2, 4, 10, 12, 18,……,100). Figure 7 gives the graphical comparison in terms of area, power and delay for the general polynomial multiplier, multiplier over irreducible trinomial and AOP based multiplier. Finally, the simplicity, regularity and modularity of bit parallel systolic multiplier using irreducible trinomial over $GF(2^m)$ architecture allow for easy extension and make this design easy to implement VLSI technologies, particularly for cryptographic application.

Table I : Comparison of three systolic multiplier over GF (2^m)

Multipliers	General polynomial multiplier	AOP based multiplier	Irreducible trinomial multiplier
Items			
Generating polynomial	General form	AOP form	Trinomial form
Array type	Systolic	Systolic	systolic
Number of cells	m^2	$(m+1)^2$	U cell - m^2, V cell –(m-1
2-input AND gate	2	1	U cell - 1, V cell - 0
2-input XOR gate	2	1	U cell - 1, V cell - 1
1-bit latches	7	3	5
Computation time per cell	$T_A + T_X$	$T_A + T_X$	$T_A + T_X$
Latency	3m	m+1	2m-1

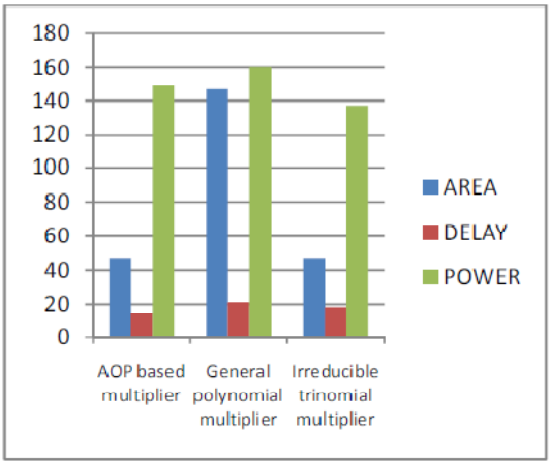

Fig. 9 : Comparison results of area, delay and power

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Implementation of CMOS Full-Adders for Energy-Efficient Arithmetic Applications

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Abstract **-** We present two high-speed and low-power full-adder cells designed with an alternative internal logic structure and pass-transistor logic styles that lead to have a reduced power-delay product (PDP). We carried out a comparison against other full-adders reported as having a low PDP, in terms of speed, power consumption and area. All the full-adders were designed with a 0.18- m CMOS technology, and were tested using a comprehensive test bench that allowed to measure the current taken from the full-adder inputs, besides the current provided from the power-supply. Post-layout simulations show that the proposed full-adders outperform its counterparts exhibiting an average PDP advantage of 80%, with only 40% of relative area.

Index Terms—*Arithmetic, full-adder, high-speed, low-power.*

I. INTRODUCTION

Energy efficiency is one of the most required features for modern electronic systems designed for high-performance and/or portable applications. In one hand, the ever increasing market segment of portable electronic devices demands the availability of low-power building blocks that enable the implementation of long-lasting battery-operated systems. On the other hand, the general trend of increasing operating frequencies and circuit complexity, in order to cope with the throughput needed in modern high-performance processing applications, requires the design of very high-speed circuits. The power-delay product (PDP) metric relates the amount of energy spent during the realization of a determined task, and stands as the more fair performance metric when comparing optimizations of a module designed and tested using different technologies, operating frequencies, and scenarios.

Addition is a fundamental arithmetic operation that is broadly used in many VLSI systems, such as application-specific digital signal processing (DSP) architectures and microprocessors. This module is the core of many arithmetic operations such as addition/subtraction, multiplication, division and address generation. As stated above, the PDP exhibited by the full-adder would affect the system's overall performance [1]. Thus, taking this fact into consideration, the design of a full-adder having low-power consumption and low propagation delay results of great interest for the implementation of modern digital systems. In this paper, we report the design and performance comparison of two full-adder cells implemented with an alternative internal logic structure, based on the multiplexing of the Boolean functions XOR/ XNOR and AND/OR, to obtain balanced delays in SUM and CARRY outputs, respectively, and pass-transistor powerless/groundless logic styles, in order to reduce power consumption. The resultant full-adders show to be more efficient on regards of power consumption and delay when compared with other ones reported previously as good candidates to build low-power arithmetic modules.

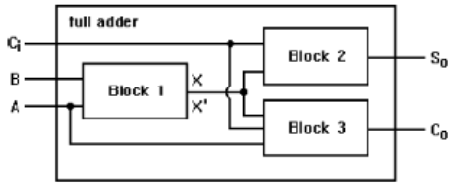

Fig. 1. Full-adder cell formed by three main logical blocks.

This paper is organized as follows. Section II presents the internal logic structure adopted as standard in previous papers for designing a full-adder cell. Section III introduces the alternative internal logic structure and the pass-transistor powerless/groundless logic styles used to build the two proposed full-adders. Section IV explains the features of the simulation environment used for the comparison carried out to obtain the power and speed performance of the full-adders. Section V reviews the results obtained from the simulations, and Section VI concludes this work.

II. PREVIOUS FULL-ADDER OPTIMIZATIONS

Many papers have been published regarding the optimization of low-power full-adders, trying different options for the logic style (standard CMOS [2], differential cascade voltage switch (DCVS) [3], complementary pass-transistor logic (CPL) [4], double pass-transistor logic (DPL) [5], swing restored CPL (SR-CPL) [6], and hybrid styles [and the logic structure used to build the adder module. The internal logic structure shown in Fig. 1 has been adopted as the standard configuration in most of the enhancements developed for the 1-bit full-adder module. In this configuration, the adder module is formed by three main logical blocks: a XOR-XNOR gate to obtain $A \oplus B$ (Block 1), $\overline{A \oplus B}$ and XOR blocks or multiplexers to obtain the SUM (*So*) and CARRY (*Co*) outputs (Blocks 2 and 3). A deep comparative study to determine the best implementation for Block 1was presented in [13], and an important conclusion was pointed out in that work: the major problem regarding the propagation delay for a full-adder built with the logic structure shown in Fig. 1, is that it is necessary to obtain an intermediate $A \oplus B$ signal and its complement, which are then used to drive other blocks to generate the final outputs. Thus, the overall propagation delay and, in most of the cases, the power consumption of the full-adder depend on the delay and voltage swing of the $A \oplus B$ signal and its complement generated within the cell. So, to increase the operational speed of the full-adder, it is necessary to develop a new logic structure that does not require the generation of intermediate signals to control the selection or transmission of other signals located on the critical path.

III. ALTERNATIVE LOGIC STRUCTURE FOR A FULL-ADDER

Examining the full-adder's true-table in Table I, it can be seen that the *So* output is equal to the $A \oplus B$ value when C=0, and it is equal to $\overline{A \oplus B}$ when C=1. Thus, a multiplexer can be used to obtain the respective value taking the C input as the selection signal. Following the same criteria, the *Co* output is equal to the A•B value when C=0 , and it is equal to A+B value when C=1. Again, C can be used to select the respective value for the required condition, driving a multiplexer. Hence, an alternative logic scheme to design a full-adder cell can be formed by a logic block to obtain the $A \oplus B$ and $\overline{A \oplus B}$ signals, another block to obtain the A•B and A+ B signals, and two multiplexers being driven by the C input to generate the So and Co outputs, as shown in Fig. 2 [13].

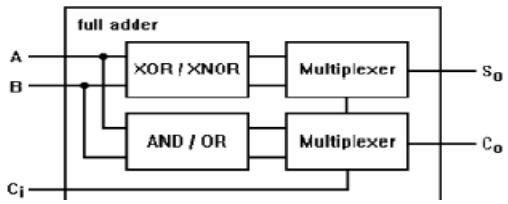

Fig. 2. Alternative logic scheme for designing full-adder cells.

TABLE I
TRUE-TABLE FOR A 1-BIT FULL-ADDER: A, B, AND C ARE INPUTS; SO AND CO ARE OUTPUTS

C	B	A	So	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The features and advantages of this logic structure are as follows.

- There are not signals generated internally that control the selection of the output multiplexers. Instead, the C input signal, exhibiting a full voltage swing and no extra delay, is used to drive the multiplexers, reducing so the overall propagation delays.
- The capacitive load for the C input has been reduced, as it is connected only to some transistor gates and no longer to some drain or source terminals, where the diffusion capacitance is becoming very large for sub-micrometer technologies. Thus, the overall delay for larger modules where the C signal falls on the critical path can be reduced.
- The propagation delay for the So and Co outputs can be tuned up individually by adjusting the XOR/XNOR and the AND/OR gates; this feature is advantageous for applications where the skew between arriving signals is critical for a proper operation (e.g., wave pipe lining), and for having well balanced propagation delays at the outputs to reduce the chance of glitches in cascaded applications.

Based on the results obtained in [13], two new full-adders have been designed using the logic styles DPL and SR-CPL, and the new logic structure presented in

Fig. 2. Fig. 3 presents a full-adder designed using a DPL logic style to build the XOR/XNOR gates, and a pass-transistor based multiplexer to obtain the So output. In Fig. 4, the SR-CPL logic style was used to build these XOR/XNOR gates. In both cases, the AND/OR gates have been built using a powerless and groundless pass-transistor configuration, respectively, and a pass-transistor based multiplexer to get the *Co* output.

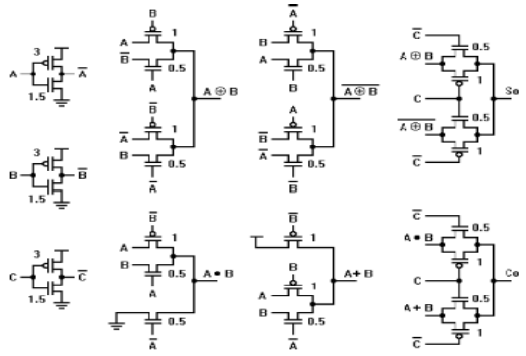

Fig. 3. Full-adder designed with the proposed logic structure and a DPL logic style (Ours1).

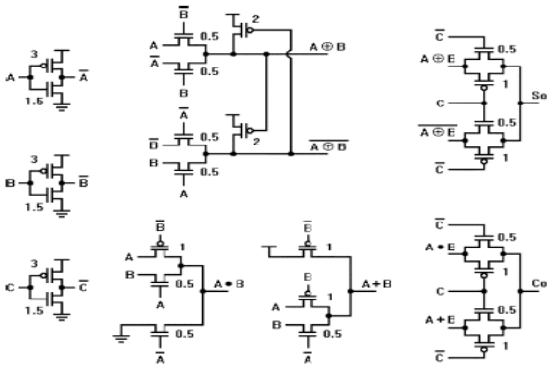

Fig. 4. Full-adder designed with the proposed logic structure and a SR-CPL logic style (Ours2).

IV. IMPLEMENTATION

Fig. 5 shows the test bed used for the performance analysis of the full-adders. This implementation has been used for comparing the full-adders analyzed in [9], [14], with the addition of the inverters at the outputs. The size of the input buffers lets to experience some degradation in the input signals, and the size of the output buffers equals the load of four small inverters for this technology. This test bed is presented as a generalization of static CMOS gates driving and been driven for the full-adder cell under test. The main advantage of using this simulation environment is that the following power components are taken into account, in addition to the dynamic one.

• The short-circuit consumption of the inverters connected to the device under test (DUT) inputs. This power consumption varies according to the capacitive load that the DUT offers at the inputs. Furthermore, the energy required to charge and discharge the DUT internal nodes when the module has no direct power supply connections (as for the case of pass-transistor logic styles), comes through these inverters connected at the DUT inputs.

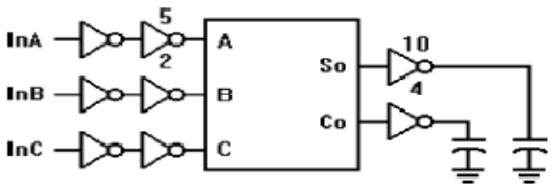

Fig. 5. Test bed used for simulating the full-adders under comparison.

• The short-circuit consumption of the DUT by itself, as it is receiving signals with finite slopes coming from the buffers connected at the inputs, instead of ideal ones coming from voltage sources.

• The short-circuit and static consumption of the inverters connected to the outputs of the DUT, which are due to the finite slopes and degraded voltage swing of the full-adder output signals. The importance of including the effects and power consumption of the buffers connected at the inputs and outputs of the DUT, comes from the fact that the DUT is always going to be used in combination with other devices to build a larger system, and these static inverters are a good generalization for any operating scenario to be considered. For the stimulus vectors, we used the test inputs patterns recommended in [1], as they exercise all the input combinations necessary to determine the worst case propagation delay and power consumption values.

V. SIMULATION RESULTS

We compared the performance of 7 full-adders, named: new14T [15], hpsc [7], hybrid [8], hybrid cmos [9], cpl [10], Ours1 and Ours2. The schematics and layouts were designed using a TSMC 0.18-□m CMOS technology, and simulated using the BSIM3v3 model (level 49)and the post-layout.

Simulations were carried out using Nanosim [16] to determine the power consumption features of the designed full-adders, and Hspice [17] to measure the

propagation delay for the output signals. In order to have a fair comparison, we took the transistors sizes for each full-adder that were reported in the correspondent paper, and made all the layouts with a homogeneous arrangement.

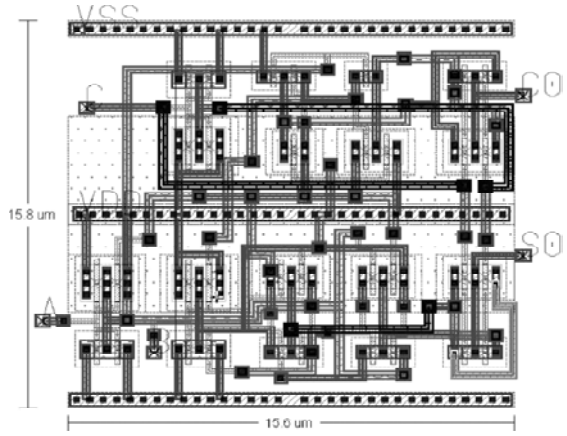

Fig. 6. Layout of the proposed full-adder Ours1

All the full-adders were supplied with 1.8 V and the maximum frequency for the inputs was 200 MHz. This table reports the results for the whole test bed (top) and for the full-adder alone (add). It is worth to observe that in some cases, the power consumed from the power-supply (pwr supply) for the full-adder is smaller than the total average power (avg power). This is because of, for some logic styles (e.g., pass-transistor style), some current is taken from the inputs of the full-adder and is used to charge the internal nodes. As mentioned above, it is the importance of considering the power consumption of the input buffers in the top test-bed. we can state the following.

• Only two full-adders exhibit static-dissipation. These are the new14T and cpl adders, which are implemented with logic styles that have an incomplete voltage swing in some internal nodes, causing this consumption component.

• The power consumption improvements of the full-adders taken in descending order correlate with the optimizations reported correspondent papers. Considering the power consumption of the whole test bench, our proposals show savings up to 60%, and considering the consumption of the standalone full-adder the savings are up to 80%. These savings can be justified by the joint reduction of dynamic and short-circuit power components.

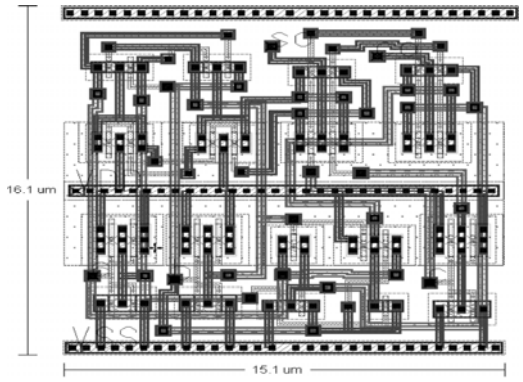

Fig. 7. Layout of the proposed full-adder Ours2.

correspondent papers. Considering the power consumption of the whole test bench, our proposals show savings up to 60%, and considering the consumption of the standalone full-adder the savings are up to 80%. These savings can be justified by the joint reduction of dynamic and short-circuit power components.

• The short-circuit consumption optimization is related to the powerless/ groundless configuration of the constituent AND/OR gates, and the dynamic consumption optimization comes from the fact of reduced capacitances in the internal nodes for pass-transistor logic styles, and for the well balanced propagation delays inside the full-adder, which results in less glitches at the outputs.

• With regards of the speed, it can be seen the advantage of the logic structure introduced here, since both realizations designed using this scheme (Ours1 and Ours2) exhibit the smallest propagation delay, only matched by the cpl full-adder. It shows a propagation delay improvement around 25% compared with the new14T and hpsc full-adders.

• The power-delay product (PDP) column confirms the energy-efficiency for the full-adders built using the new internal logic structure. They present the lowest PDP metric, up to 85% of saving, due to the combined reduction of power consumption and propagation delay.

• In addition, we carried out separated simulations to determine the lowest power supply voltage that each full-adder can tolerate, while keeping its correct functionality. As shown in column “Vdd min”, the proposed full-adders can operate properly with voltage supplies as low as 0.6 V. Since these realizations have neither static consumption, nor internal direct paths from Vdd to Gnd (except for the inverters at the inputs, which could be avoided if the inputs come from FF’s with complementary outputs), they are good candidates

for battery-operated applications where low consumption modules with standby modes are required.

• The importance of the simulation setup and the inclusion of the power consumption components for the surrounding circuitry are evident, as some realizations reported previously as low-power cells have been shown to perform worse than other ones when considering the power consumption of the whole test-bed.

• On regards of the implementation area obtained from the layouts, it can be seen that the proposed full-adders require the smallest area (up to 40% of relative area), which can also be considered as one of the factors for presenting lower delay and power consumption, as it implies smaller parasitic capacitances being driven inside the full-adder. The reason for the smaller area, compared to other full-adders that have less transistors, is that the size of the transistors in the proposed full-adders is minimal and not larger than 2 □m (except for the symmetrical response inverters at the

inputs), while for other full-adders the transistor sizes are in the range of 4 to 6 □m. Figs. 6 and 7 show the layouts of the proposed full-adders, with the correspondent side by side dimensions.

• Finally, we determined the maximum frequency that each full adder can operate, while being supplied with 1.8 V. The proposed full-adders reach up to 1.25 GHz, only surpassed by cpl cell, at the expense of major power consumption and area. The reason for running the power-delay performance simulations at 200 MHz was due to the full adders that work only up to 250 MHz.

V. I OUTPUT WAVEFORMS

In fig. 7.1 the simulation results for this full adder Hybrid CMOS has shown in this waveform as all inputs are applying with same rise time, fall time, pulse value and frequency. Hence the three inputs are merged into single waveform. It can be observed in the first waveform. The simulation is carried out at 200 MHZ frequency. Post layout simulation for this full adder shows the overall power dissipation is 102.5 nano watts. The delay is 182.7 pico seconds for sum output and 149 pico seconds for carry output. The average delay for this full adder is 145.3 pico seconds

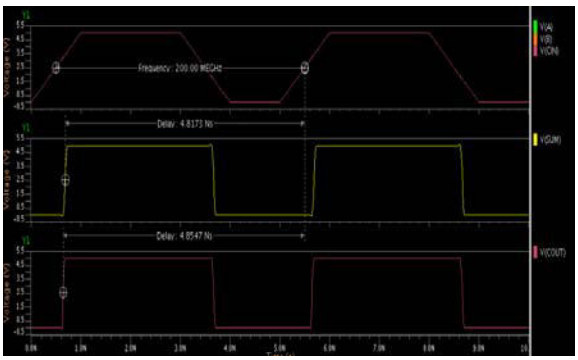

Fig 7.1 Output waveforms of the HYBRID CMOS full adder

VI. CONCLUSION

An alternative internal logic structure for designing full-adder cells was introduced. In order to demonstrate its advantages, two full-adders were built in combination with pass-transistor powerless/groundless logic styles. They were designed with a TSMC 0.18-□m CMOS technology, and were simulated and compared against other energy-efficient full-adders reported recently. H spice and Nano sim simulations showed power savings up to 80%, and speed improvements up to 25%, for a joint optimization of 85% for the PDP. The area utilization for the proposed full-adders is only 40% of the largest full-adder compared, and the power-supply voltage for the proposed full-adders can be lowered down to 0.6 V, maintaining proper functionality.

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Effects of Excitation System and Power System Stabiliser Parameters on Power System Transient Stability

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Abstract - The Transient stability of an Electrical Power system is greatly influenced by the Excitation Controller and Power System Stabilizer parameters. In this paper, both these effects are analyzed in detail using a very easy, accurate and reliable Simulink setup developed for this purpose. This helps in the design and analysis of Transient response of a typical power system designing the parameters of these systems to get a desired Transient response. The method suggested in this work is very general and can be applied to any system in a quick time with high accuracy and reliability.

Keywords - *Transient stability, Excitation, Stabilizer, Infinite bus system, Torque.*

I. INTRODUCTION

The stability of an Electrical Power System has always been a serious problem and required lot of attention from Power Engineers. The Stability of a power System can be defined as its ability to continue to supply Load with quality and un-interrupted power to the consumers. The stability is mainly classified as steady state stability and Transient stability. The steady state stability involves small signal deviations whereas, Transient stability deals with large deviations resulting from large and sudden changes in the operating conditions. The Transient stability limit of a power system is less than steady state stability limit[2].

The Electrical power system actually comprises of many generators and other components and hence represents a complicated system for analysis. Under the influence of disturbances, there will be imbalances between mechanical input and Electrical output resulting in oscillations. These oscillations are divided into local modes (1-2Hz) and inter area modes (0.4-0.7Hz)[1]. In cases where analysis is required for local modes, the power system can be considered as a single machine infinite bus system (SMIB). Hence, in this work, the analysis involving Excitation Controller and Power System Stabilizer is carried out considering only SMIB. The details of the SMIB considered in this paper are contained in APPENDIX I.

II. EXCITATION CONTROLLER

In this work, the effect of Excitation controller is examined and the system considered is as shown in Fig1. In this work, the limits contained in the Fig are ignored.

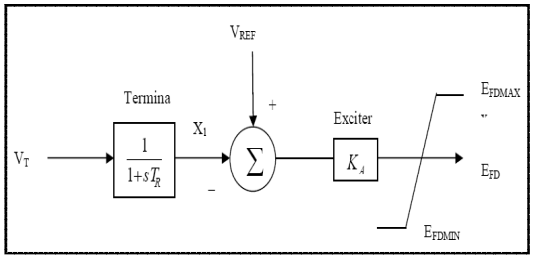

Fig. 1

To study the effect of any controller, small signal analysis is done and the necessary state variable representation elements are derived.[1] the values of these elements are derived from the given system contained in the Appendix1. The state variable representation is shown in equation 1.The time responses of this system are shown in Figs 2 and 3.

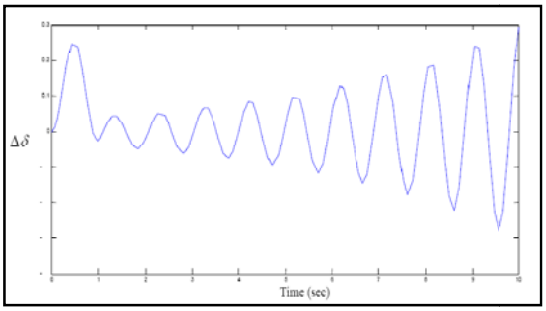

Fig. 2

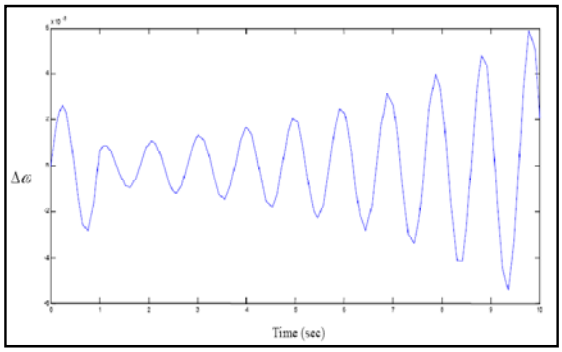

Fig. 3

The parameters taken in this work has been used and the elements of the state variable representation as given in equation (1) are evaluated along with its Eigen values to determine the small signal stability. From the Eigen values, as given in APPENDIX III, it is seen that the time response is unstable and this can further be justified by the time responses as given in Figs 2 and 3.

The block diagram representation of SMIB is shown in Fig 4.

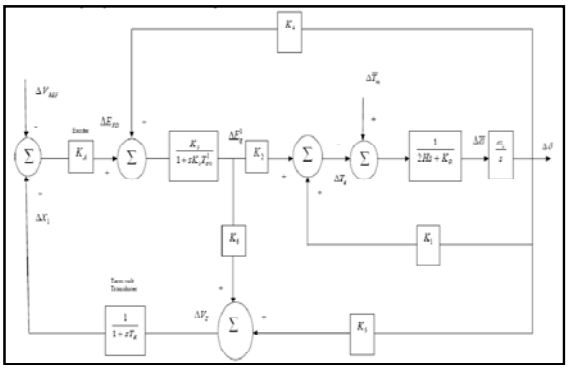

Fig. 4

The block diagram representation of SMIB with exciter and PSS is shown in Fig 5

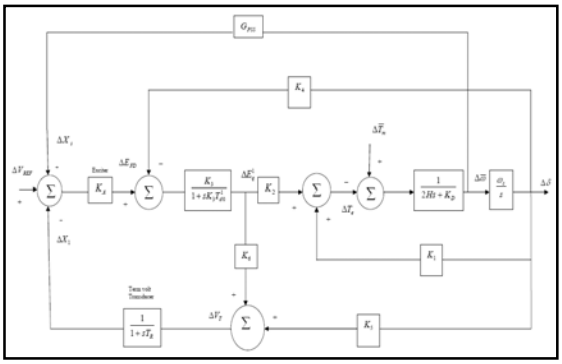

Fig. 5

The state variable representation of SMIB with PSS is shown in equation 2 and its Eigen values are given in APPENDIX IV.

The block diagram of the Power System stabilizer is shown in Fig 6.

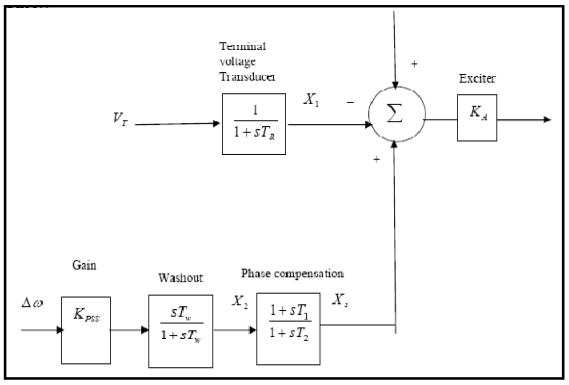

Fig. 6

The time responses of this system with the inclusion of the above shown Power System Stabilizer are shown in Figs 7 and 8.

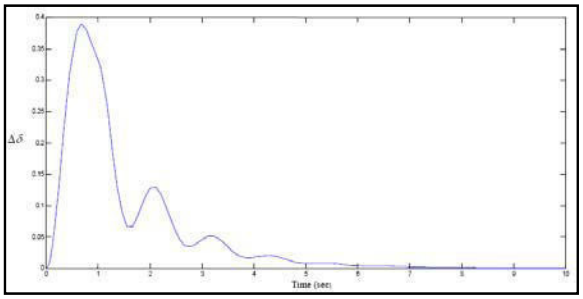

Fig. 7

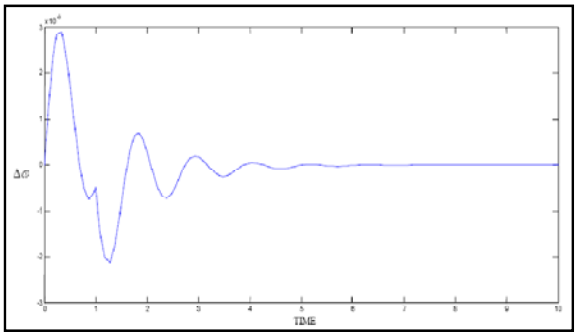

Fig. 8

To the SMIB power System considered earlier, the Power System stabilizer has been included and the resulting state variable representation is shown as equation (2). To this representation, the parameter values as given in the APENDIX II are used and the

Eigen values are calculated which are given in APPENDIX IV. From these Eigen values, it is seen that the power system stability under small oscillation has improved from the previous one and in fact, it has become stable as seen from the time responses shown in Figs 7 and 8.

III. DETAILS OF SIMULINK SETUPS

The SIMULINK setups developed in this work is shown in Figs 9 and 10.

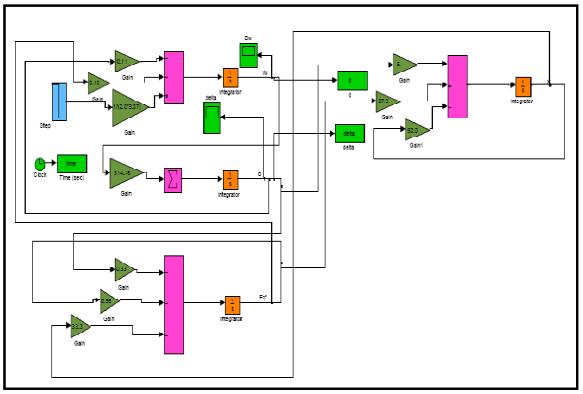

Fig 9: Simulink Setup For SMIB Suitable For Small Signal Analysis With Excitation Controller

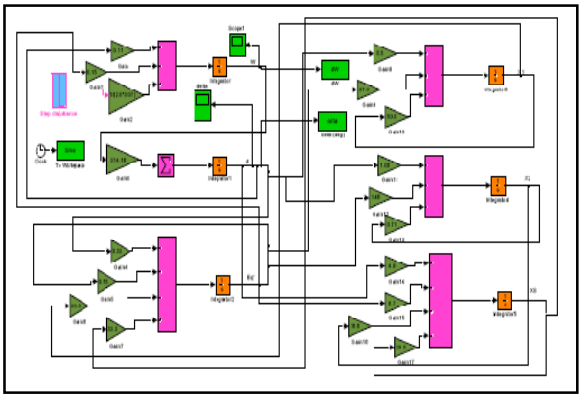

Fig 10: Simulink Setup For SMIB Suitable For Small Signal Analysis With Excitor And Power System Stabilizer

IV. STRUCTURE OF POWER SYSTEM STABILIZER

The block diagram of power system stabilizer is shown in figure.6 which consists basically of three major blocks.

a) Gain.

b) Phase compensation

c) Signal washout.

The gain of the PSS can be adjusted to ensure satisfactory and desired response of the generator for all types of transients expected and is usually tuned at site.

Phase compensation block provides necessary phase lead to compensate for phase lag between exciter input generator electrical (air–gap) torque. Phase compensation is required for a frequency range of 0.1-2 Hz and usually, the phase lead provided is a compromised value to ensure satisfactory operation for different operating conditions. To prevent negative synchronizing torque component, the phase lag between exciter input and electrical torque is under – compensated.

The signal washout is a high pass filter to let in rotor oscillation without magnitude reduction. It prevents steady changes in speed modifying terminal voltage and ensures that PSS responds only to changes in speed. The value of the time constant T_W is anywhere between 1 to 20 seconds. The exact value is not critical. On the whole, PSS improves overall system stability as is shown in this work

$$\begin{bmatrix} \Delta\dot{\omega} \\ \Delta\dot{\delta} \\ \Delta\dot{E}_q^1 \\ \Delta\dot{X}_1 \end{bmatrix} = \begin{bmatrix} \frac{-K_D}{2H} & \frac{-K_1}{2H} & \frac{-K_2}{2H} & 0 \\ \omega_S & 0 & 0 & 0 \\ 0 & \frac{-K_4}{T_{d0}^1} & \frac{-1}{k_3 T_{d0}^1} & \frac{-K_A}{T_{d0}^1} \\ 0 & \frac{-K_5}{T_R} & \frac{K_4}{T_R} & \frac{-1}{T_R} \end{bmatrix} \begin{bmatrix} \Delta\omega \\ \Delta\delta \\ \Delta Eq' \\ \Delta X_1 \end{bmatrix} + \begin{bmatrix} \Delta T_m \\ 0 \\ \left(\frac{K_A}{T_{d0}^1}\right)\Delta V_{REF} \\ 0 \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} \Delta\dot{\omega} \\ \Delta\dot{\delta} \\ \Delta\dot{E}_q^1 \\ \Delta\dot{X}_1 \\ \Delta\dot{X}_2 \\ \Delta\dot{X}_3 \end{bmatrix} = \begin{bmatrix} \frac{-K_D}{2H} & \frac{-K_1}{2H} & \frac{-K_2}{2H} & 0 & 0 & 0 \\ \omega_S & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{-K_4}{T_{d0}^{'}} & \frac{-1}{K_3 T_{d0}^{'}} & \frac{-K_A}{T_{d0}^{'}} & 0 & \frac{K_A}{T_{d0}^{'}} \\ 0 & \frac{K_5}{T_R} & \frac{K_6}{T_R} & \frac{-1}{T_R} & 0 & 0 \\ a & b & c & 0 & \frac{-1}{T_W} & 0 \\ \frac{aT_1}{T_2} & \frac{bT_1}{T_2} & \frac{cT_1}{T_2} & 0 & d & \frac{-1}{T_2} \end{bmatrix} \begin{bmatrix} \Delta\omega \\ \Delta\delta \\ \Delta E_q^{'} \\ \Delta X_1 \\ \Delta X_2 \\ \Delta X_3 \end{bmatrix} + \begin{bmatrix} \frac{\Delta T_m}{2H} \\ 0 \\ \frac{K_A}{T_{d0}^1}\Delta V_{REF} \\ 0 \\ \frac{K_{PSS}}{2H}\Delta T_m \\ \frac{K_{PSS}}{2H}\Delta T_m \frac{T_1}{T_2} \end{bmatrix} \quad (2)$$

Where

$$a = -\frac{-K_{PSS}K_D}{2H} \quad b = \frac{-K_{PSS}K_1}{2H} \quad c = \frac{-K_{PSS}K_2}{2H} \quad d = -\left(\frac{T_1}{T_2}\right)\left(\frac{1}{T_W}\right) + \frac{1}{T_2}$$

V. CONCLUSION

In this work, a SMIB power system is analyzed for small signal stability for a total time period of 10 sec. For the parameters of the system selected, the state variable matrix is evaluated and their Eigen values are determined. From these values, the time response is obtained using a simulink setup developed for this work. From this it is seen that the system is unstable. The

original system with exciter is added to a power system stabilizer and with selected parameters; the state variable representation matrix is again obtained. From the Eigen values obtained from this matrix, the time response is obtained using the developed simulink setup and the original system which was unstable, became stable. The procedure of implementation and use of the simulink setups is very general, accurate and easy for implementation and the small signal stability for any power system for chosen parameters can be obtained. In this way, using the procedure indicated, the desired time response can be obtained using the developed simulink setups.

APPENDIX I

Generator rating	588MVA
H	3.07
X_d	2.35
X_d'	0.253
X_e	0.65
V_t	1.0
δ_o	80.58^o
KD	0.0
T_{dO}'	6.0
P_O	0.85
Q_O	0.52 (lagging)

APPENDIX II

$K_{PSS} = 9.5$

$T_W = 1.4$

$T_1 = 0.154$

$T_2 = 0.0335$

APPENDIX III

$\lambda_1 = 0.2276+j\ 6.552$

$\lambda_2 = 0.2276 - j\ 6.552$

$\lambda_3 = -25.5044+j17.4875$

$\lambda_4 = -25.5044-j17.4875$

APPENDIX IV

$\lambda_1 = -35.9239$

$\lambda_2 = -0.7442$

$\lambda_3 = -1.0239+j\ 5.6635$

$\lambda_4 = -1.0239-j\ 5.6635$

$\lambda_5 = -21.2015+j\ 23.2415$

$\lambda_6 = -21.2015-j\ 23.2415$

ACKNOWLEDGEMENTS

The Authors are thankful to the managements of C.V.R. College of Engineering, Hyderabad and JNT University, Hyderabad, for providing facilities and to publish this work.

NOMENCLATURE

δ	Torque angle
ω	Angular Frequency
H	Inertia constant
E_{FD}	Exciter output voltage
K_A	Gain of the exciter
T_A	Time constant of the exciter
V_T	Generator terminal voltage
X_d'	Generator transient reactance
K_D	Damping gain
Δ	Small signal variation
T_{dO}'	Direct axis open-circuit time constant.
$K_1, K_2, \ldots\ldots K_6$	Constants of the single-machine infinite bus system.
V_{REF}	Reference voltage of the Excitation system.
T_R	Terminal voltage transducer time constant.
K_{PSS}	Gain of the power system stabilizer.
T_W	Washout time constant of the power system stabilizer.
T_1, T_2	Phase compensation time constants of the power system stabilizer.
X_1, X_2, X_S	Signals of the power system stabilizer.
E_q'	Generator voltage.
ω_S	Synchronous radian frequency.
T_m	Mechanical torque.
X_e	Reactance between machine and the load.

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Effect of Surface Passivation on the Electrical Characterization of Ge/Al203/Al Moscaps

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***Abstract* -** Two types of passivation techniques are investigated on Germanium Moscaps- Chlorine and Sulphur passivation. N2 annealing is done after dielectric deposition and metallization. Sulphur passivated samples showed higher accumulation capacitance and better EOT whereas Chlorine passivated samples showed lesser leakage current.

***Keywords* -** *Passivation, EOT(Equivalent Oxide Thickness), ISD(Interface State Density), Leakage current, RTP(Rapid Thermal Processing), PVD(Physical Vapour Deposition), PDA(Post Deposition Annealing), PMA(Post Metallization Annealing),ALD(Atomic Layer Deposition).*

I. INTRODUCTION

It is well known that high K dielectrics are replacing SiO2 as gate dielectric for conventional CMOS application [1]. CMOS Scaling of SiO2 below 10A˚ results in high leakage current due to tunnelling which exemplifies the need for high K dielectric. Al203 has been considered as one of the potential candidates either by itself or in combination with Hf02 over the last decade [9]. Al203 has high bandgap(~8.7eV) and good thermal stability which ensures low leakage current[9]. Renewed interest in Ge as a material of choice for future electronics is mainly due to its attractive properties, including the lower effective mass and higher mobility of carriers for increasing drive current capability of MOSFETs, and smaller optical band gap for broader absorption wavelength spectrum [2].In addition, the process developments(ALD, optimization etc..) in high-*k* gate dielectric over the last few years has increased the possibility of high-*k*/Ge system to be implemented for future gate stack. However, several years studies on high-*k*/Si system indicate that tremendous efforts should be paid on the high-*k* interface engineering in order to achieve successful scaling of EOT with low-leakage current, good subthreshold characteristics, high carrier mobility, and acceptable reliability [2]. The interfaces with either the gate or the Si channel region are particularly important in regard to device performance [3]. These regions, serve as a transition between the atoms associated with the materials in the gate electrode, gate dielectric and Si channel [3]. These interface regions (Fig. 1) can alter the overall capacitance of the gate stack, particularly if they have a thickness which is substantial relative to the gate dielectric. The effect of these interfacial regions is reduced by passivation and annealing.Previous passivation studies include Si, Ge – F passivation, O3, Forming gas passivation etc...

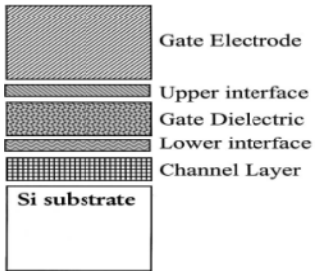

Fig. 1 : Schematic of important regions of a field effect transistor gate stack.

II. EXPERIMENTS

The diameter of the n-doped (Sb) Ge wafer with <100> orientation is 50.8mm and its resistivity is 1~10 ohm-cm. Two such wafers were subjected to passivation treatment- one with Chlorine and other with Sulphur. Sulphur passivation was done by dipping the wafer in (NH4)2S solution at 50˚C for 20 minutes. Chlorine passivation was done by dipping the wafer in 20% HCl solution for 2minutes.Al203 of thickness 10nm was deposited on these passivated samples using PVD chamber (AMAT ENDURA).The dielectric deposition was done at room temperature and at a pressure of 1.87mT. The 02 and Ar flow rates were 25sccm and 10sccm respectively. The RF power used was 500W. Dielectric deposition was followed by PDA at 400˚C, for 2minutes using RTP system . 100nm thick Al gate was then deposited using thermal evaporator employing shadow mask of diameter 400µm. PMA was done at 400˚C using RTP system. Electrical characterization

included CV and IV analysis were done using the probe stations. From the obtained plots, ISD (using conductance method) and EOT were calculated. Dit was calculted using conductance method. The film quality was ensured using ellipsometry.

III. RESULTS AND DISCUSSION

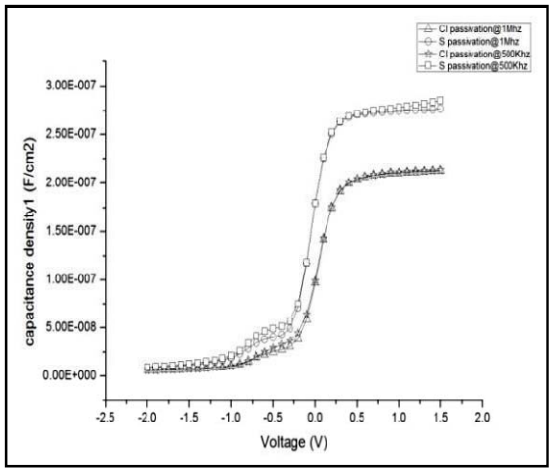

Fig. 2 : CV Plots of S and Cl passivated samples at 500Khz and1Mhz.

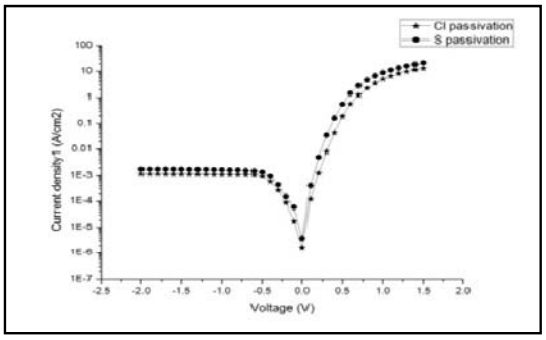

Fig. 3 : JV plot of S and Cl passivated samples

Fig. 2 shows the CV characteristics of S and Cl passivated samples at 2 different frequencies. It can be seen that S passvn shows better capacitance at both 500 KHz and 1 MHz respectively. Leakage is marginally lower due to possibly thicker interface. CV also shows a kink near Vfb, probably due to high interface state density. Interface State densities were found to be 6.96*1012/ cm2 and4.46*1011/ cm2 for Sulphur and Chlorine passivated samples respectively.

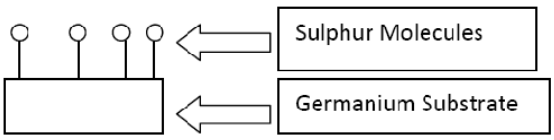

Fig. 4 : Sulphur molecules passivating the Germanium surface

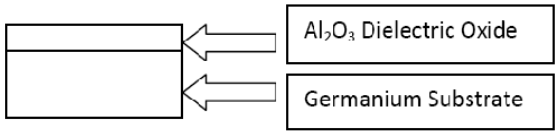

Fig. 5 : Germanium Moscap with Sulphur passivation after PDA

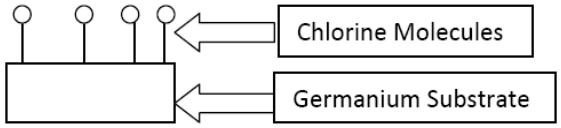

Fig 6. Chlorine molecules passivating the Germanium surface

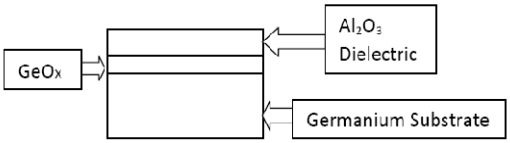

Fig 7. Germanium Moscap with Chlorine passivation after PDA

During sulphur passivation(Figure4), Germanium surfaces were terminated with sulphur molecules that replaced the dangling bonds .These sulphur molecules are stable and they remain on the surface for a longer time. After PDA (Figure 5), majority of the sulphur molecules are replaced with Al203 molecules and some of the sulphur molecules still remain, that creates more interface traps. But in case of chlorine passivation (Figure6), the chlorine molecules are not able to satisfy all the dangling bonds completely. As such a layer of Ge0x is being formed every 10 minutes [4].After the dielectric deposition and PDA (Figure 7), there is a chance of increase in the amount of Ge0x. The Ge/Ge0x layer is much stable compared to Ge/Al203 layer, formed in the sulphur passivation. It is evident that as the thickness of the film layer in chlorine passivated samples is greater when compared to the sulphur passivated samples, the capacitance value decreases for chlorine passivated samples. From figure 3, it is evident that the leakage current is less for chlorine passivated samples when compared to sulphur passivated samples.

IV. CONCLUSIONS

Passivation results that we obtained reveals that Sulphur is the best passivating agent compared to chlorine passivation.The reason is that Sulphur passivation gives higher accumulation capacitance when compared to Chlorine passivation. Also with the

application of passivation, leakage current is reduced significantly.

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Synchronous Reference Frame Based Control Strategy For Three-Phase Four-Wire(3P4W) Unified Power Quality Conditioner (UPQC)

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Abstract - This paper presents a new synchronous reference frame (SRF) based control method to compensate the power quality problems through a three-phase four-wire (3P4W) unified power quality conditioner (UPQC) under unbalanced and distorted load conditions. The proposed UPQC system can improve the power quality at the point of common coupling (PCC) on power distribution system under unbalanced and distorted load conditions. The simulation results based on MATLAB Simulink are discussed in detail to support the SRF based control method presented in the paper.

Keywords - *Unified Power Quality Conditioner (UPQC), Synchronous Reference Frame (SRF), active power filter, power quality.*

I. INTRODUCTION

Unified power quality conditioner systems were widely studied by many researchers as an eventual method to improve power quality in the electrical distribution systems [1-11]. The aim of unified power quality conditioner is to eliminate the disturbances that affect the performance of the critical load in power system. The UPQC, therefore, is expected to be one of the most powerful solutions to large capacity loads sensitive to supply voltage imbalance distortions [3]. The UPQC, which has two inverters that share one dc link, can compensate the voltage sag and swell, the harmonic current and voltage, and it can control the power flow and voltage stability. Besides, the UPQC with the combination of a series Active Power Filter (APF) and a shunt APF can also compensate the voltage interruption if it has some energy storage or battery in the dc link [4]. The shunt APF is usually connected across the loads to compensate for all current-related problems, such as the reactive power compensation; power factor improvement, current harmonic compensation, neutral current compensation, regulate the dc-link voltage and load unbalance compensation, whereas the series APF is connected in a series with a line through series transformer. It acts as a controlled voltage source and can compensate all voltage-related problems, such as voltage harmonics, voltage sag, voltage swell, flicker, etc.[2], [3].

In this paper, the proposed SRF based control method source voltage and source current are measured, evaluated and tested under unbalanced and distorted load conditions.

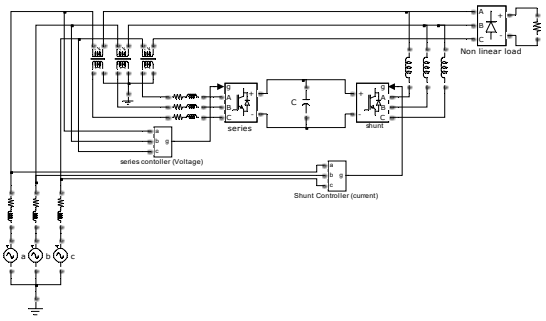


Fig. 1: Block Diagram of UPQC

II. UNIFIED POWER QUALITY CONDITIONER

The UPQC for harmonic elimination and simultaneous compensation of voltage and current, which improve the power quality, offered for other harmonic sensitive loads at the PCC. Almost all of the papers on UPQC, it is shown that the UPQC can be utilized to solve PQ (power quality) problems simultaneously [12-15].

Fig. 1 shows a basic system configuration of a general UPQC with series APF and shunt APF. The main aim of the series active power filter is to obtain harmonic isolation between the load and supply. It has capability of voltage imbalance compensation as well as voltage regulation and harmonic compensation at the utility-consumer PCC. The shunt APF is used to absorb current harmonics, to compensate for reactive power and to regulate the dc-link voltage between both active power filters.

III. THE SYNCHRONOUS REFERENCE FRAME

The SRF method can be used to extract the harmonics contained in the supply voltages or currents. For current harmonic compensation, the distorted currents are first transferred into two-phase stationary coordinates using α-β transformation (same as in p-q theory). After that, the stationary frame quantities are transferred into synchronous rotating frame using cosine and sinus functions from the phase locked loop (PLL). The sinus and cosine functions help to maintain the synchronization with supply voltage and current. Similar to the p-q theory, using filters, the harmonics and fundamental components are separated easily and transferred back to the a-b-c frame as reference signals for the filter. The SRF algorithm is also known as d-q method, and it is based on a-b-c to d-q-0 transformation (park transformation), proposed for active filter compensation [13]. Several APF and UPQC application works presented in the literature is about improving the performance of the compensator [14-20].

In the SRF based active power filter applications in 3P4W system voltage and current signals are transformed into the conventional rotating frame (d-q-0). In the SRF method, the transformation angle (ωt) represents the angular position of the reference frame which is rotating at the constant speed in synchronism with three-phase ac voltage. In nonlinear load condition, harmonics and reactive currents of the load are determined by PLL algorithms. Then currents with the same magnitude and reverse phase are produced and injected to the power system in order to compensate neutral current, harmonics and reactive power. In the stationary reference frame, α-β-0 coordinates are stationary, while in the synchronous reference frame, d-q-0 coordinates rotate synchronously with supply voltages. Thus, the angular position of supply voltage vector shows the angular position of the synchronous reference frame [13-20].

In 3P4W systems, since id component of the current in ―d coordinate is in phase with voltage, it corresponds to the positive sequence current. However, i_q component of the current in ―q coordinate is orthogonal to i_d component of the current, and it corresponds to negative sequence reactive current. The i_0 component of the current, which is orthogonal to i_d and i_q, corresponds to zero sequence component of the current. If i_q component of the current is negative, the load has inductive reactive power. If it is positive, the load has capacitive reactive power. In 3P4W nonlinear power systems $_{id}$ and i_q components of the current include both oscillating components and average components.

The oscillating components of the current correspond to harmonic currents and average components of the current correspond to active and reactive currents [13, 14, 20]. In the balanced and linear three-phase systems, the load voltage and current signals generally consist of fundamental positive sequence components. However, in unbalanced and nonlinear load conditions, they include fundamental positive, negative and zero sequence components. In active power filter applications, the fundamental positive sequence components of the signals should be separated in order to compensate harmonics.

IV. SRF BASED CONTROL ALGORITHM

Among the several APF control methods presented in the literature, the SRF based control method is one of the most conventional and the most practical methods [11,12] [14-17] The SRF method presents excellent characteristics but it requires decisive PLL techniques.

The sensing of only source current to realize SRF based or other type controller for shunt APF is not new and this kind of the controller can be found in the literature [22].

A. Reference voltage signal generation for series APF

The SRF based UPQC control algorithm can be used to solve the power quality problems related with source voltage harmonics, unbalanced voltages and voltage sag and swell at the same time for series APF. In this method, the series APF controller calculates the reference value to be injected by the series transformers, comparing the positive-sequence component of the source voltages with load side line voltages. In equation, the supply voltages V_{Sabc} are transformed d-q-0 by using transformation matrix **T** given in equation.

The instantaneous source voltages (v_{Sd} and v_{Sq}) include both oscillating components and average components under unbalanced source voltage with harmonics. Oscillating components of v_{Sd} and v_{Sq} consist of the harmonics and negative sequence components of the source voltages under distorted load conditions.

$$T = \sqrt{\frac{2}{3}}\begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ \sin(wt) & \sin(wt-\frac{2\pi}{3}) & \sin(wt+\frac{2\pi}{3}) \\ \cos(wt) & \cos(wt-\frac{2\pi}{3}) & \cos(wt+\frac{2\pi}{3}) \end{bmatrix} \quad (1)$$

$$T^{-1} = \sqrt{\frac{2}{3}}\begin{bmatrix} \frac{1}{\sqrt{2}} & \sin(wt) & \cos(wt) \\ \frac{1}{\sqrt{2}} & \sin(wt-\frac{2\pi}{3}) & \cos(wt-\frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \sin(wt+\frac{2\pi}{3}) & \cos(wt+\frac{2\pi}{3}) \end{bmatrix} \quad (2)$$

$$\begin{bmatrix} v_{S0} \\ v_{Sd} \\ v_{Sq} \end{bmatrix} = \mathrm{T} \begin{bmatrix} v_{Sa} \\ v_{Sb} \\ v_{Sc} \end{bmatrix} \quad (3)$$

These component is then filter through LPF and then again transformed V_{Sabc} using inverse transformation matrix $\mathbf{T^{-1}}$ given in above equation after that apply to pulse width modulation (PWM) controller to produce IGBT switching signals and to compensate all voltage-related problems, such as voltage harmonics, sag, swell and voltage unbalance, etc. at the PCC.

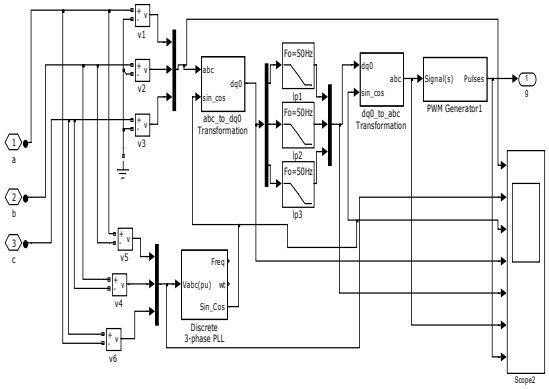
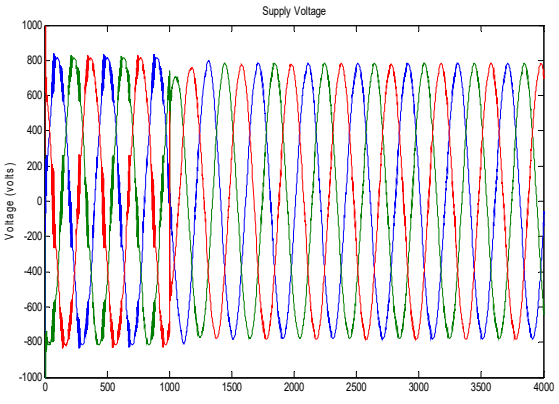


Fig. 2 : Control Strategy for Series Active Filter



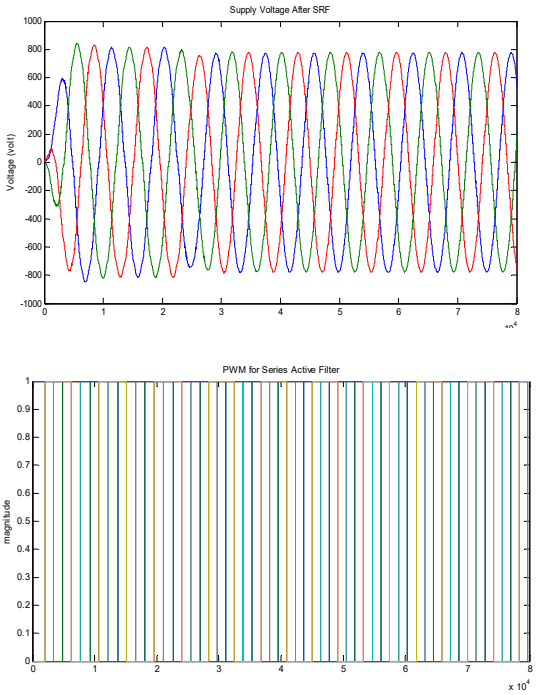


Fig. 3 : Output Of PWM for Series Active Filter

B. Reference source current signal generation for shunt APF

The shunt APF described in this paper is used to compensate the current harmonics generated in the nonlinear load and the reactive power. The proposed SRF based shunt APF reference source current signal generation algorithm uses only source voltages, source currents and dc-link voltages. The source currents are transformed to d-q-0 coordinates using transformation matrix **T** given in equation. In 3P4W system and nonlinear load condition, the instantaneous source currents (i_{Sd} and i_{Sq}) include both oscillating components and average components[21]. The oscillating components consist of harmonic and negative sequence components of the source currents. The average components consist of positive sequence components of current and correspond to reactive currents. These component is then filter through LPF and then again transformed I_{Sabc} using inverse transformation matrix $\mathbf{T^{-1}}$ given in above equation after that apply to pulse width modulation (PWM) controller to produce IGBT switching signals and to compensate all current-related problems, at the PCC.

$$\begin{bmatrix} i_{S0} \\ i_{Sd} \\ i_{Sq} \end{bmatrix} = \mathrm{T} \begin{bmatrix} i_{Sa} \\ i_{Sb} \\ i_{Sc} \end{bmatrix} \quad (4)$$

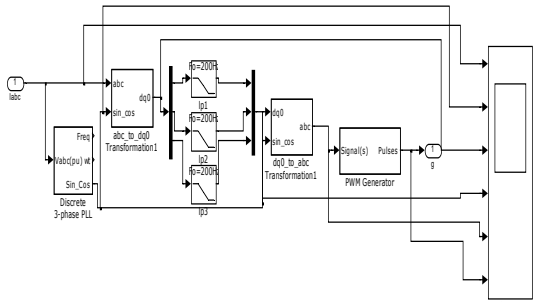


Fig. 4 : Control Strategy for Shunt Active Filter

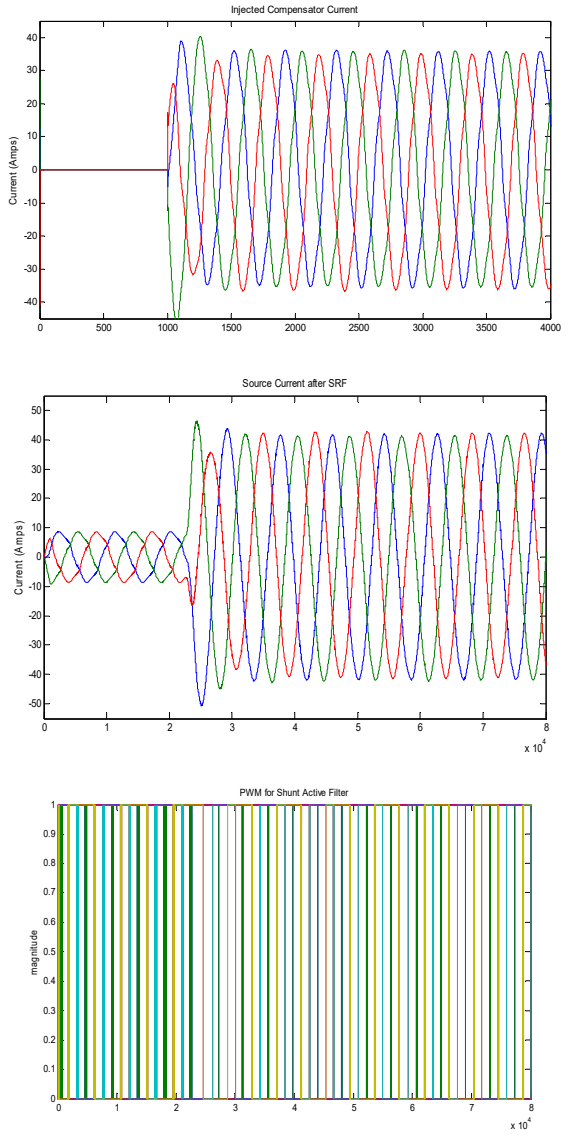


Fig. 5: Output Of PWM for Shunt Active Filter

V. SIMULATION RESULTS

In this study, the SRF based control algorithm for the UPQC is evaluated by Matlab/Simulink software under unbalanced and distorted load current and source voltage conditions since the unbalanced load currents are very common and yet an important problem in 3P4W distribution system. The UPQC system parameters used in this study are given in Table. In the simulation studies, the results are specified before and after the operation of the UPQC system. The passive filters with R and C are used to remove the switching ripple in the voltage and current waveforms. Finally, the voltage and current harmonic compensation capability of the UPQC. The THD levels are given before and after filter operated under SRF method. The obtained results show that this control method allows THD level of currents and voltages by mitigation of all harmonic components.

In the SRF based control algorithm, mains currents (i_{Sabc}) and voltages (v_{Sabc}) are measured to calculate shunt APF reference current; and the mains and load voltages (v_{Labc}) are used in series APF controller. Parameter for UPQC is as follow :

PARAMETERS	VALUE
Source:	
Voltage	1000V
Frequency	50Hz
3-phase resistance	0.001 Ω
3-phase inductance	10mH
Load resistance	100Ω
DC Link:	
Voltage	2100V
Capacitor	0.01mF
Series active filter:	
Switching frequency	12kHz
Filter resister	0.01Ω
Filter inductance	5H
Series transformer	2kVA
Shunt active filter:	
Switching frequency	1.08kHz
AC line inductance	0.1H

THD levels before and after UPQC.

Signal	Before UPQC	After UPQC
Supply	14.47	2.48
Load **voltage**	14.72	13.52
Supply	17.17	6.57
Load current	17.17	6.64

The control algorithm has the ability of compensating both harmonics and reactive power of the load eliminated. This control method has been evaluated and tested under steady-state load conditions.

The current and voltage with distortion is compensated to create the sinusoidal waveforms at the PCC. The harmonics and unbalanced components are compensated excellently in case of unbalanced and distorted current and voltage at the PCC. Simulation results show that the SRF control strategy compensates to harmonic components as well as most of the other unbalanced load current distortions. It is shown that the UPQC can compensate the voltage and the current problems simultaneously and it has excellent compensating characteristics even when the unbalanced components occur, in electric power systems with the 3P4W[23].Simulation results of the SRF based control method for before & after UPQC are as below

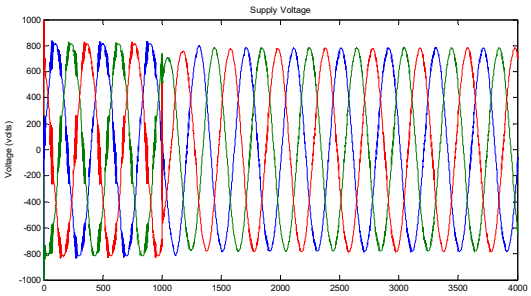


Fig. 6 : Supply Voltage

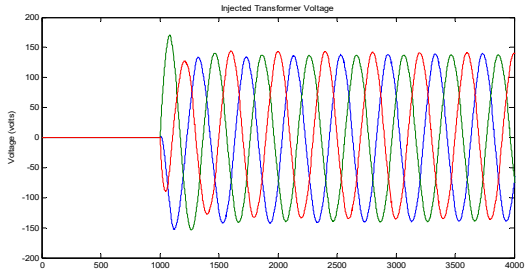


Fig. 7 : injected transformer voltages

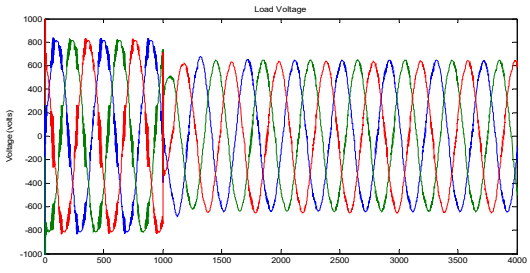


Fig. 8 : Load Voltages

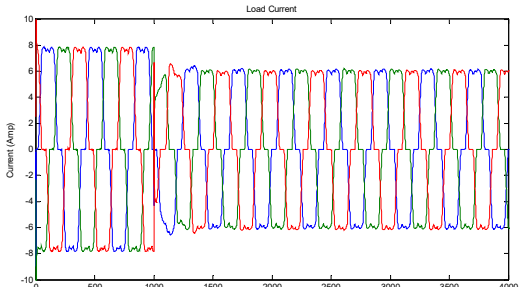


Fig. 9 : Load Current

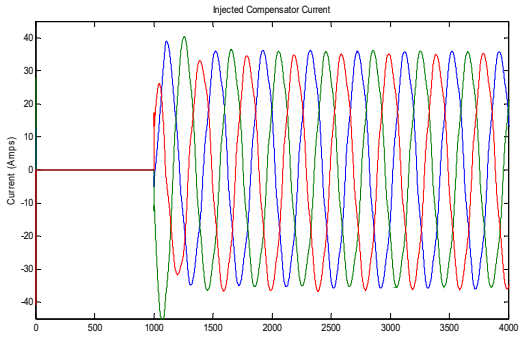


Fig. 10 : Injected Compensator Current

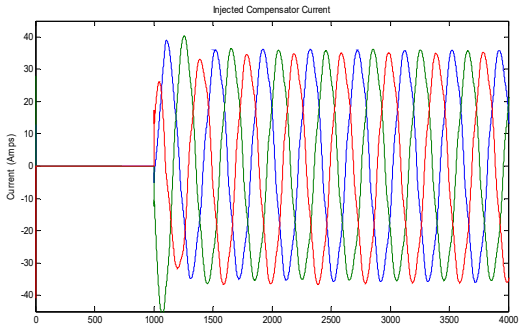


Fig. 11: Source Current

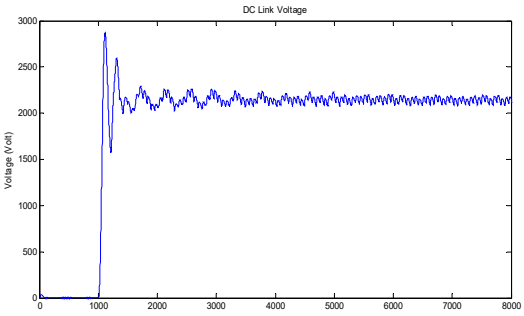


Fig. 12: DC Link Voltages

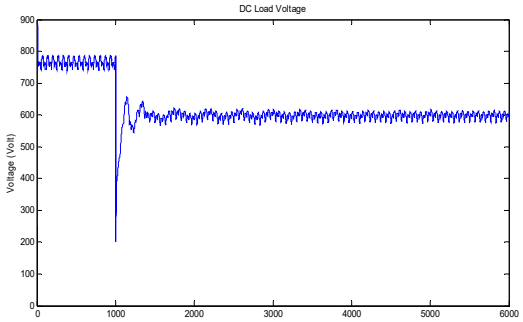


Fig. 13: DC Load Voltage

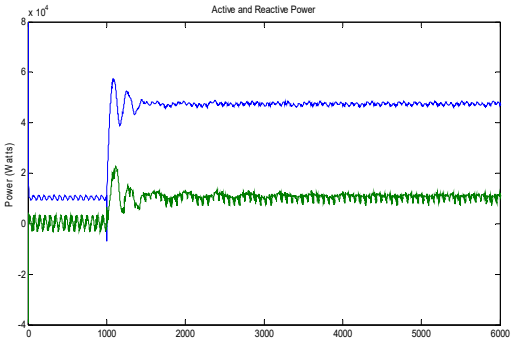


Fig. 14: Active and Reactive Power

As shown in the results, the proposed control strategy provides better dynamic responses to load current variation and so the stability of the UPQC control is enhanced. As a result, the proposed method is very effective and successful in harmonic compensation under unbalanced and distorted load condition as shown in simulation results.

VI. CONCLUSION

This paper describes a SRF based control strategy used in the UPQC, which mainly compensates the reactive power along with voltage and current harmonics under non-ideal mains voltage and unbalanced load current conditions. The proposed control strategy uses only loads and mains voltage measurements for the series APF, based on the synchronous reference frame theory. This methods require the measurements of load, source and filter currents for the shunt APF and source and injection transformer voltage for the series APF. The simulation results show that, when unbalanced and nonlinear load current condition, the above control algorithm eliminates the impact of distortion and unbalance of load current on the power line, making the power factor unity. Meanwhile, the series APF isolates the loads and source voltage in unbalanced and distorted load condition, the shunt APF compensates reactive power, and harmonics, and provides three-phase balanced and rated currents for the mains.

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Modeling and Simulation of Fuel Cell and Microturbine as Distributed Generators in a Microgrid

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Abstract **-** As energy consumption rises, one must find a suitable alternative for generation of electrical energy to supplement conventional existing generation facilities. In this regard, distributed generation (DG) will continue to play a critical role in the energy supply demand. The common technologies available as DG are micro-turbines, solar photovoltaic systems, fuel cells stack and wind energy systems. This paper presents a dynamic model of two important distributed generators, Fuel Cell and Microturbine. In order to investigate the ability of Fuel Cell and Microturbine units in distribution system, their efficient modeling is required. The model is developed in the MATLAB/Simulink software.

Keywords- *Fuel Cell, Microturbine, Distributed generation, Dynamic model.*

I. INTRODUCTION

Distributed generation (DG) is not a new concept but is an emerging approach for providing electric power in the heart of the power system. It mainly depends upon the installation and operation of a group of small size, compact, and clean electric power generating units at or near an electrical load (consumer). Till now, not all DG technologies and types are economic, clean or reliable. In general, DG's are defined as the supply to the consumers through small-scale electricity generation. There is not a consistent definition that can describe DG technology. DGs are defined according to its name, purpose, location rating etc [1].

Usually DGs are classified according to their operating technologies. However, it is more convenient to classify them from the electric point of view to study their impact on the electric system. Different classifications can be obtained to differentiate between DG types according to their electrical applications, supply duration, generated power types, electric ratings and renewable and non-renewable technologies. Several proposed DG classification will be discussed as follows.

Distributed Generation is expected to play a major role in future power generation systems. DG can help reduce transmission losses, improve power quality to end users, and smooth peaks in demand patterns. Fuel cells and micro turbines are the dominant distributed energy recourses used in DG. These two resources are combined to build an integrated system for best economic operations.

Fuel cells produce dc voltage outputs, and they are connected to electric power networks through power conditioning units such as DC/AC converters. Fuel cells have slow transient response and slow output power ramping thus cannot follow loads effectively. A grid connected fuel cell needs to have a battery, which would make up for the differences between the required voltage and the full cell output voltage. The combined fuel cell / battery can provide good voltage support and reactive power compensation.

Micro turbines are small and simple cycle gas turbines with outputs ranging from 25 kW to 300 kW. They are one part of general evolution of gas turbine technology. Turbine speeds mainly range from 50000 rpm to 120000 rpm. The other types of micro turbine is a split shaft design that uses power turbine rotating at 3600 rpm and a conventional generator connected through a gearbox.

In a combined fuel cell and micro turbine system the fuel cell controls the voltage magnitude and the reactive power compensation while the gas turbine provides the bulk of load following. This paper presents the modeling of a grid-connected fuel cell. The Solid Oxide Fuel Cell (SOFC) is considered in this study. A SOFC has faster transient response than other types of fuel cells.

Here the modeling of micro turbine and fuel cell plant is modeled and simulated using Matlab/Simulink software package.

II. SOLID OXIDE FUEL CELL

Fuel cells are electro-chemical devices and are used to convert the chemical energy of a gaseous fuel directly into electricity. In fuel cells, a chemical reaction takes place to convert hydrogen and oxygen into water and releasing electrons in the process. A fuel cell consists of two electrodes, known as the anode and cathode that are separated by an electrolyte as shown in Figure 1. Oxygen is passed over the cathode and hydrogen over the anode. Hydrogen ions are formed together with electrons at the anode and migrate to the cathode through the electrolyte. Electrons then flow to the electrode through an external circuit [2].

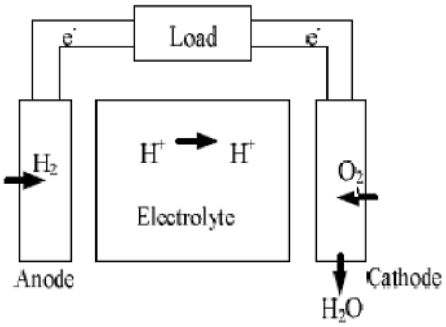

Fig. 1: Schematic diagram of fuel cell

In this thesis, the solid oxide fuel cell (SOFC) is considered in the development of the fuel cell model. It is suitable for large stationary power generation, relatively simple and responds quickly to load changes. The dynamic model is based on the following chemical and physical principles:

1) Electrochemical model: Component material balance equations;
2) Thermal model: Energy balance equations;
3) Voltage activation, concentration, and ohmic losses: Nernst voltage equation.

A. Overall Chemical Reaction

The overall electrochemical reaction that occurs inside the fuel cell is given by the following equations.

Anode side reaction: $H_2 \rightarrow 2H^+ + 2e^-$ (1)

Cathode side reaction: $1/2O_2 + 2H^+ + 2e^- \rightarrow H_2O + Heat$ (2)

Overall reaction: $H_2 + 1/2O_2 \rightarrow H_2O + Heat$ (3)

The component balance equation for the various components such as fuel, air, water is given

$$\frac{PV}{RT} T_S \frac{dx_i}{dt} = W_i^{in} - W_i^{out} - R_i \quad (4)$$

where P is the Pressure of the cell (P), V the volume of stack(m^3), x_i the molarity of species(no units), W_i^{in} the inflow rate of species (moles/sec), W_i^{out} the outflow rate of species (moles/sec), R_i the reaction rate (moles/sec), i = 1,2,3 represents the species fuel, air, water respectively[3].

B. Power Conditioning

A Power Conditioning Unit (PCU) connects a fuel cell power plant to the power grid. Applying the Pulse Width Modulation (PWM) technique to the converter allows the fuel cell with a controllable ac-voltage with fundamental frequency given by:

$$V_{ac} = m \angle V \angle \delta \quad (5)$$

Where V is the dc voltage at fuel cell terminal, m is the amplitude modulation index of the converter, and δ is the firing angle of PCU with respect to the phase angle of the bus voltage.

As mentioned earlier in the introduction, the fuel cell needs a battery to make up for the slow transients. Figure 2 shows the block diagram that contains fuel cell, battery, battery interface, and PCU connected to the grid.

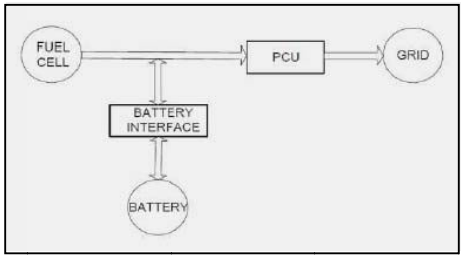

Fig. 2: Block diagram of fuel cell with PCU

C. Mathematical Model of the Solid Oxide fuel Cell

The SOFC model is derived by considering the total stack voltage of the fuel cell stack which is given by,

$$V = N_0 \left[E_0 + \frac{RT}{2F} \left(\ln \frac{P_{H_2} P_{O_2}^{1/2}}{P_{H_2O}} \right) \right] - rI \quad (6)$$

Where,

V : Total stack voltage (V)
E_0 : Standard reversible cell potential (V)
r : Internal resistance of stack (Ω)
I : Stack current (A)
N_0 : Number of cells in stack
R : Universal gas constant (J/ mol K)
T : Stack temperature (K)
F : Faraday's constant (C/mol)

P_{H2} : Partial pressure of hydrogen (Pa)

P_{o2} : Partial pressure of oxygen (Pa)

P_{H2O} : Partial pressure of water (Pa)

rI : ohmic loss of the stack(V)

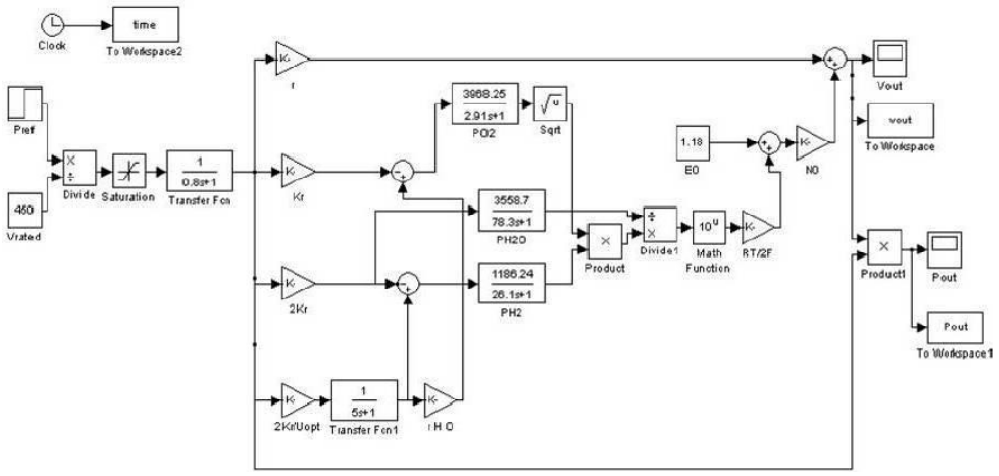

Fig. 3 : SOFC model in MATLAB

For the dynamics of the SOFC, consider the partial pressure of hydrogen, oxygen and water given in equations (7), (8) and (9), respectively. The slow dynamics of the fuel cell current (I) is represented by equation (10).

$$P_{H_2} = \left(\frac{1/K_H}{1+\tau_{H_2}s}\right)(qH_2 - 2KrI) \quad (7)$$

$$P_{O_2} = \left(\frac{1/K_{O_2}}{1+\tau_{O_2}s}\right)(qO_2 - KrI) \quad (8)$$

$$P_{H_2O} = \left(\frac{1/K_{H_2O}}{1+\tau_{H_2O}s}\right)(2KrI) \quad (9)$$

$$I = \left(\frac{I_{ref}}{1+\tau_e s}\right) \quad (10)$$

I_{ref} is the reference current which is given by equation (11). The fuel and oxygen flows are given by equations (12) and (13).

$$I_{ref} = \left(\frac{P_{ref}}{V_{fc}}\right) \quad (11)$$

$$qH_2 = \left(\frac{2K_r}{U_{opt}}\right)\left(\frac{1}{1+\tau_f s}\right) \quad (12)$$

$$qO_2 = \frac{qH_2}{rHO} \quad (13)$$

Parameter	Value
Operating Temperature(T)	1273 K
Faraday's Constant(F)	96487 C/mol
Universal Gas Constant(R)	8314 J/k mol K
Standard Reversible Cell Potential(E)	1.18 V
Number of Cells(N)	381
Constant(Kr =N/4F)	$9.87\text{x}10^{-4}$
Valve Molar Constant of Hydrogen(K_{H_2})	$8.43\text{x}10^{-6}$kmol/s atm
Valve Molar Constant of Oxygen(K_{O_2})	$2.81\text{x}10^{-4}$kmol/s atm
Valve Molar Constant of Water(K_{H_2O})	$2.52\text{x}10^{-5}$ k mol/ s atm
Response Time for Hydrogen Flow (τ_{H_2})	26.1 s
Response Time for Water Flow (τ_{H_2O})	78.3 s
Response Time for Oxygen Flow(τ_{O_2})	2.91 s
Ohmic loss(r)	0.126 Ω
Electrical Response Time (τ_e)	0.8 s
Fuel Processor Response Time(τ_f)	5 s
Ratio of Hydrogen to Oxygen(rHO)	1.145
Optimum Fuel Utilization (U_{opt})	0.85
Base MVA	100

Table 1: Parameters used in SOFC simulation

Using the above equations, a dynamic simulation model of SOFC is developed using the MATLAB/ Simulink program as shown in Figure 3. The parameters of the simulation model of fuel cell are given in Table 1. [4][5].

D. Evaluation

Figure 4 shows the stack voltage which reaches a steady state value of 400V in 5.8s. Figure 5 show stack current of the fuel cell which takes 5.8s to reach a steady state value of 25A. Figure 6 shows the response of the fuel cell for a commanded real power of 10kW. The slow response of the fuel cell is due to slow electrochemical reactions in the cell. The chemical response in the fuel processor is usually slow. This dynamic response function is modeled as a first order transfer function with a 5 sec time constant. The electrical response time in the fuel cell is fast and mainly associated with the speed at which the chemical reaction is capable of restoring the charge that has been drained by the load. This dynamic response function is also modeled as the first order transfer function with a 0.8 sec time constant.

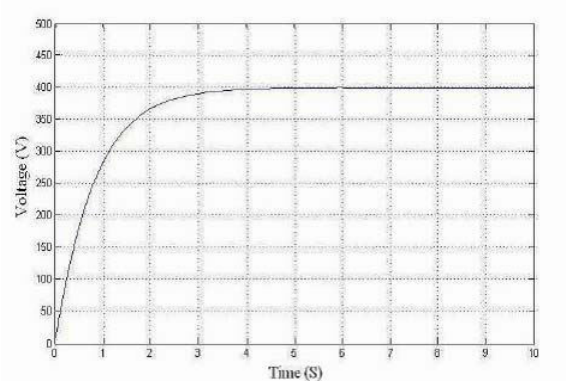

Fig.4 : Fuel Cell Output Voltage

The stack current in Figure 5 is limited based on the utilization range. The fuel utilization is initially high and gradually settles at an optimum value of 0.85. Figure 6 shows the stack power which takes 5.8s to reach the commanded value of 10kW.

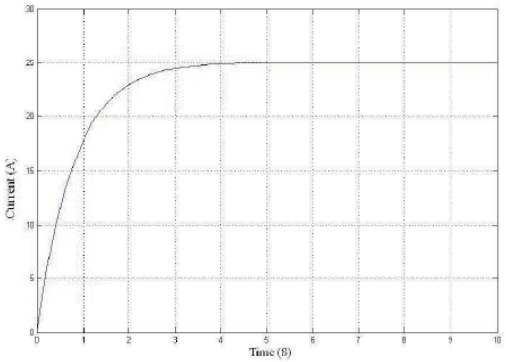

Fig. 5 : Stack Current

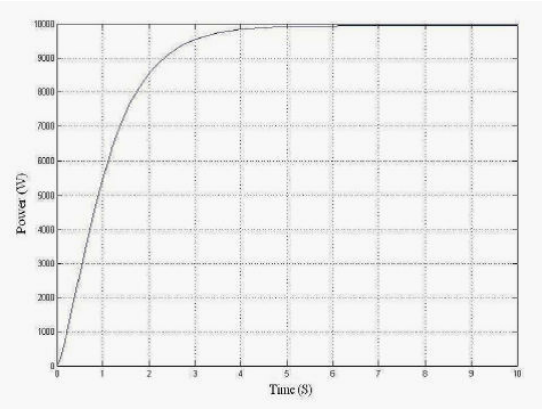

Fig. 6 : Fuel Cell Output Power

From the simulation result, it is clear that the SOFC has some slow dynamic response, so that using SOFC alone may be not suitable for system that need fast dynamic response. Hence the Microturbine can be used with the SOFC to deal with a fast system response.

III. MICRO-TURBINE (MT)

Micro turbines are small capacity combustion turbines, which can operate using natural gas, propane, and fuel oil. In a simple form, they consist of a compressor, combustor, recuperator, small turbine, and generator. MTs are small scale of 0.4–1m3 in volume and 20–500kW in size. Micro-turbines were derived from turbocharger technologies found in large trucks or the turbines in aircraft auxiliary power units (APUs). Micro-turbines will run at less temperature and pressure and faster speed (90,000 to 120,000 rpm) and sometimes they require no gearbox. However, a few manufacturers have developed alternative systems with multiple stages and/or lower rotation speeds.[6].

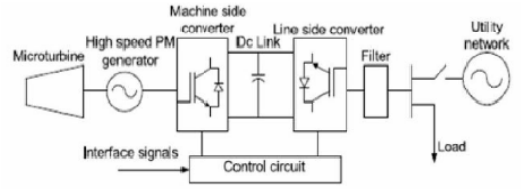

Fig. 7: Microturbine generator system configuration

The simplified single shaft gas turbine including all its control systems which is implemented in Simulink of the MATLAB is shown in Figure 8. The model consists of temperature control, fuel control, turbine dynamics, speed governor and acceleration control blocks. The model presented in this paper concentrates on the slow dynamics of the micro turbine generation (MTG) system. It is assumed that the system is operating under normal operating conditions by neglecting fast dynamics

of the Microturbine (e.g., start-up, shutdown, internal faults and loss of power).

The speed control operates on the speed error formed between a reference speed and the MTG system rotor speed. It is the primary means of control for the microturbine under part load conditions. Speed control is usually modeled by using a lead-lag transfer function or by a PID controller. In this work a lead lag transfer function has been used to represent the speed controller. The governor controls are shown in the Figure.8 with parameters gain, X, Y and Z which can be adjusted so that the governor can act with droop or as isochronous governor. Acceleration control is used primarily during turbine startup to limit the rate of the rotor acceleration prior to reaching operating speed. If the operating speed of the system is close to its rated speed, the acceleration control could be eliminated in the modeling.

The output of the governor goes to a low value select to produce a value for Vce, the fuel demand signal. The other signal into the low value select is from the temperature controller. The per unit value for Vce, corresponds directly to the per unit value of mechanical power on turbine base in steady state. The fuel flow controls as function of Vce, are shown in a series of blocks including the valve position and flow dynamics. The value of Vce, is scaled by the gain value of 0.77 and offset by a value represented by the fuel flow at no load that is rated speed condition. The time delay preceding the fuel flow controls represents the delays in the governor control using digital logic in place of analog devices.

The fuel burned in the combustor results in turbine torque and exhaust gas temperature is measured by a thermocouple. The output from the thermocouple is compared with a reference value. Normally the reference value is higher than the thermocouple output and this forces the output from the temperature control to stay on the maximum limit permitting uninhibited governor/speed control.

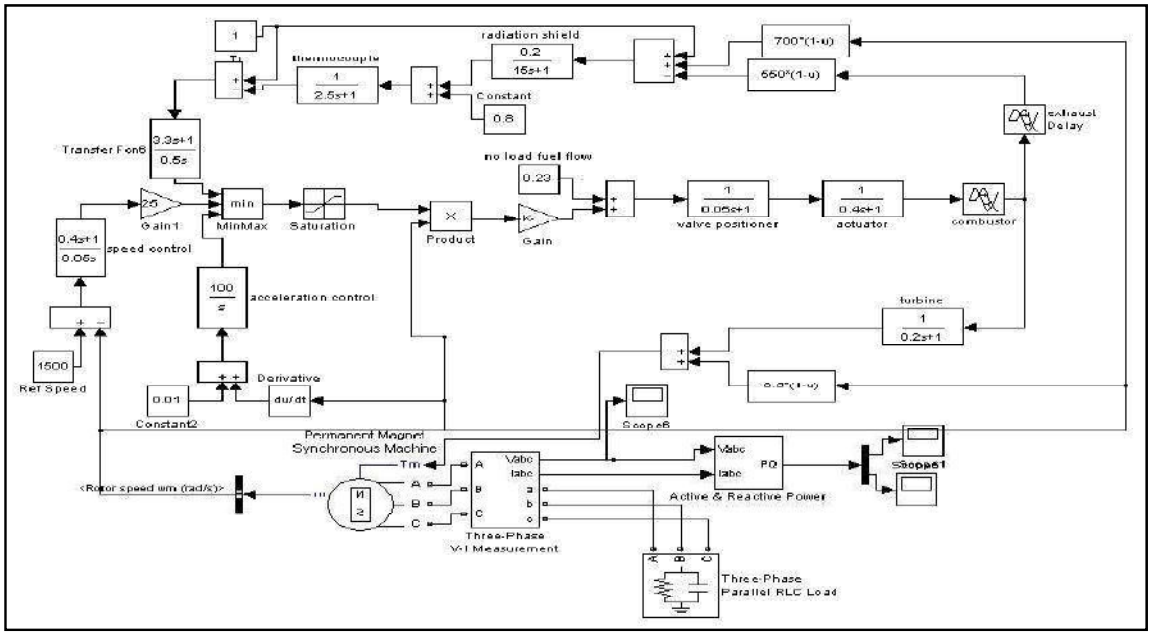

Fig.8. Simulink implementation of microturbine system.

When the thermocouple output exceeds the reference temperature, the difference becomes negative and it starts lowering the temperature control output. When the temperature control output becomes lower than the governor output, the former value will pass through the low value select to limit the output, and the unit will operate on temperature control [7].

A. Permanent Magnet Synchronous Machine

The model adopted for the generator is a 2 pole permanent magnet synchronous machine (PMSM) with a non-salient rotor. At 1600 Hertz (96 000 rpm), the machine output power is 10 kW and its terminal line-to-line voltage is 400 V. The electrical and mechanical parts of the machine are each represented by a second-order state-space model. The model assumes that the flux established by the permanent magnets in the stator is sinusoidal, which implies that electromotive forces

are sinusoidal. The following equations expressed in the rotor reference frame (dq frame) are used to implement PM synchronous machine.

Electrical equations:

$$\frac{d}{dt}i_d = \frac{1}{L_d}v_d - \frac{R}{L_d}i_d + \frac{L_q}{L_d}pw_r i_q \quad (14)$$

$$\frac{d}{dt}i_q = \frac{1}{L_q}v_q - \frac{R}{L_q}i_q - \frac{L_d}{L_q}pw_r i_d - \frac{\lambda pw_r}{L_q} \quad (15)$$

$$T_e = 1.5p(\lambda i_q + (L_d - L_q)i_d i_q) \quad (16)$$

Mechanical equations:

$$\frac{d}{dt}w_r = \frac{1}{J}(T_e - Fw_r - T_M) \quad (17)$$

$$\frac{d}{dt}\theta = w_r \quad (18)$$

Where

L_q , L_d : q and d axis inductances(H)

R : Resistance of the stator windings (Ω)

i_q , i_d : q and d axis currents (I)

v_q , v_d : q and d axis voltages (V)

w_r : Angular velocity of the rotor (rad/sec)

λ : Flux induced by the permanent magnets in the stator windings. (wb)

p : Number of pole pairs

T_e : Electromagnetic torque (N/m)

J : Combined inertia of rotor and load (N)

F : Combined viscous friction of rotor and load (N)

θ : Rotor angular position (Degree)

T_M : Shaft mechanical torque. (Nm)

B. Evaluation

Figure 8 shows the simulation model implemented in the SimPowerSystems of the MATLAB to study the performance of the MTG system operation in grid connected mode. The utility network, to which the MTG system is connected, is represented by a RC load. The micro turbine generation system takes speed of the PMSM as input. The torque output of the microturbine is given as an input mechanical torque (*TM*) to the PMSM. The direction of the torque *TM*, is positive during motoring mode and made negative during generating mode of the PMSM.

Parameter	Value
Rated power (Prate)	10 kW
Rated voltage (Vrated)	400 V
Proportional gain in PI control(KP)	1
Integral gain in PI control(Ki) Damping of turbine(Dtur)	1.08 0.03
Fuel system lag time constant 1 (T1)	10.0 s
Fuel system lag time 2(T2)	0.1 s
Load limit time constant(T3)	3.0 s
Load limit(Lmax)	1.2
Maximum value position(Vmax)	1.2
Minimum value position(Vmin)	-0.1
Temperature control loop gain(KT)	1
Number of poles(p)	2
Resistance of stationary part(RS)	0.1Ω
Resistance of rotor circuit referred to the stationary circuit(Rr)	0.1Ω
Inductance of stationary circuit(LS)	0.0059 H
Inductance of rotor circuit referred to the stationary circuit(Lr)	0.0059 H
Mutual inductance(Lm)	0.2037 H
Damping of generator(Dgen) Generator inertia(J)	0.1 0.02 kg.m
Generator friction(F)	0.0057 N.m.s

Table 2: Parameters used in MT simulation

It is important to evaluate the appropriateness of the developed models for our system studies. Here, we make some observations based on the stand-alone dynamic performance of the split-shaft microturbine model. Assume a split-shaft microturbine system is operating with constant rated voltage 400 V and power demand 10 kW. All parameters are the same as in Table 2. [8]

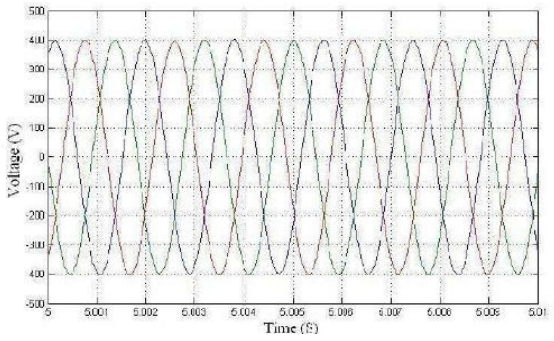

Fig. 9 : Out put voltage of Microturbine

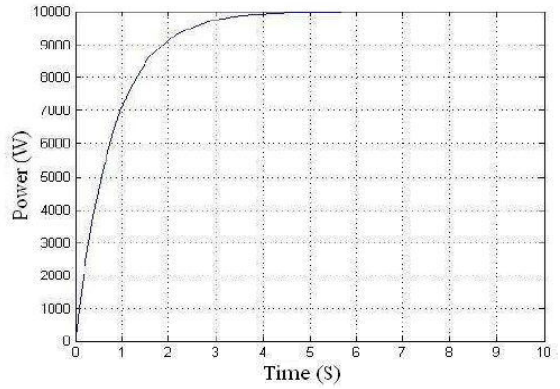

Fig. 10 : Out put Power of Microturbine

IV. CONCLUSIONS

In this paper, a simplified slow dynamic model of split-shaft microturbines is developed. In addition, an integrated SOFC system model is expanded by defining appropriate control systems and parameters for the time frame of interest. Evaluations of these stand-alone models show that they are reasonable and suitable for slow dynamic simulations. A distribution system with some simple but practical control strategies is developed for the analysis of load-following service provided by microturbines and fuel cell systems. It is demonstrated that microturbines and fuel cells are capable of providing load-following service in the distribution system.

In future, it is planned to design and analise the performance of fuel cell and microturbine when connected to grid.

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DSTATCOM Devices Connected to Distribution Systems for Dynamic Improvement of AC Generators By Voltage Control Method

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Abstract - Presently distribution generation and devices based on power electronics. This contribution starts from the dynamic study about the AC generators (Induction and synchronous machines) and distribution static synchronous compensator devices. In this context An AC generator have received more attention it is known that such machines draws very large reactive current during fault condition and gets down the mesh voltage and conduct voltage instability. A solution of this problem need a dynamic reactive power compensation .For this work the DSTATCOM is very much suitable. The behavior of DSTATCOM is improving the voltage stability performance of distribution system with AC generator (induction generator). Two control strategy of a DSTATCOM are adopted power factor controller and voltage control which may adversely affect the stability performance of synchronous generators. DSTATCOM is simulated through a model for a controllable three phase voltage source which has suitable stability studies.

Keywords - *AC Generators, DSTATCOM, Voltage stability, Distributed generation, custom power devices.*

I. INTRODUCTION

Distributed generation is a small scale electricity generation. It is fairly a new concept in electric energy market. Electric utilities are seeking new technologies to provide acceptable power quality and reliability. Current power distribution systems are receiving increased installation of distributed generation. For improving power quality and reliability custom power devices have been adopted. But more attention has been given to the equipment based on the voltage source converter technology. Distribution static synchronous compensator (DSTATCOM) is the best example of this type of devices .Distribution static synchronous compensator (DSTATCOM) improve the voltage stability performance of distribution system with induction generators is investigated. Such investigation based on three phase non- linear dynamics. Simulation utilizing the power system blocks set for use with matlab simulink. For analysis of a DSTATCOM two control strategy adopt –

1. Voltage control,
2. Power factor control.

For such studies a DSTATCOM is represented by a model based on controllable three-phase voltage sources and an algebraic model of DC link. The main impact on the stability performance of distribution network due to simultaneous usage of ac generators and DSTATCOM devices are determined.

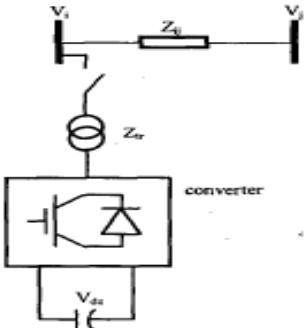
II. INDUCTION GENERATORS

An Induction generator is identical in electrical and mechanical construction to induction motor. A motor is normally wound for a voltage somewhat below the nominal system voltage drop caused by motors load current. An Induction generator is an Induction motor which is driven above the generators speed by a suitable prime mover and is provided a source of sufficient reactive power for excitation. The induction generator is very simple, reliable and low cost so it is well suited for many industrial applications. Here we discuss about the dynamic behavior of the induction generator and it is represented for a sixth order three phase model in the dq rotor reference frame .In first case the simulated without DSTATCOM, a three phase capacitor bank was connected to the terminal of the induction generator, which was fixed to keep the terminal voltage at 1p.u. during steady state. In this case the mechanical power was considered constant (i.e. the effect of prime mover and governor were neglected. The synchronous generator was represented by an eight order three-phase model in the d-q rotor reference frame such a generator was equipped with an AVR Automatic voltage regulator . The mechanical power was considered constant. And all electrical variable and parameters are referred to the stator.

III. DSTATCOM Devices

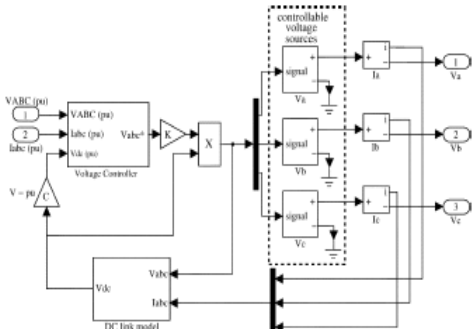
A DSTATCOM consist of a three phase voltage source converter which is shunt connected to the distribution network. DSTATCOM is the most

important device for distribution network. It has been widely used since the 1990's to precisely regulate system voltage improve voltage profile, reduce voltage harmonics, reduce transmit voltage disturbances and load compensation. The DSTATCOM uses a power electronic converter to synthesis the reactive power output. A DSTATCOM converter is controlled using pulse width modulation PWM. In Distribution voltage level devices, the employed switching element is the IGBT (Integrated Gate Bipolar Transistor), due to its lower switching losses and reduced size. The PWM (Pulse width Modulation) control the output voltage and eliminate the harmonic component. Consequently the output voltage control may be executed through the pulse width modulation PWM switching method .For this analysis the performance of DSTATCOM devices acting either a voltage controller or a power factor controller. It is assumed that the converter is directly controlled.



A directly controlled converter is more difficult and expensive to implement than an indirectly controlled converter, the former presents superior dynamic performance. DSTATCOM devices can be represented by a controllable three phase voltage source behind a transformer as a shown in figure. Here Va , Vb, Vc represent the reference instantaneous voltage to the converter in pu, which is determined from the control signal Vabc. And the output voltage of the converter in volts and dependent of the dc link voltage .

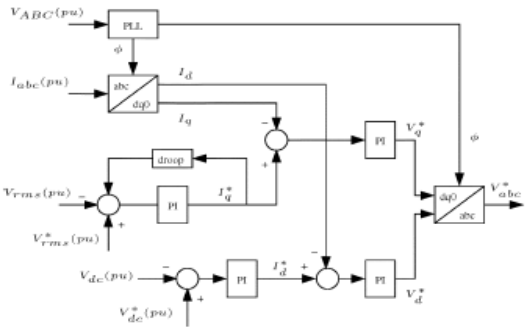
Therefore it is important to represent the DC link dynamics. This can be built based on the energy conversion principle. The AC output terminal must always be equal as per energy conservation principle ,can be expressed mathematically Vdc and Idc are the voltage and current in the dc link , and Iabc are the currents injected into the network by the DSTATCOM.



DSTATCOM Structure (Generalize)

IV. DSTATCOM Voltage Controller

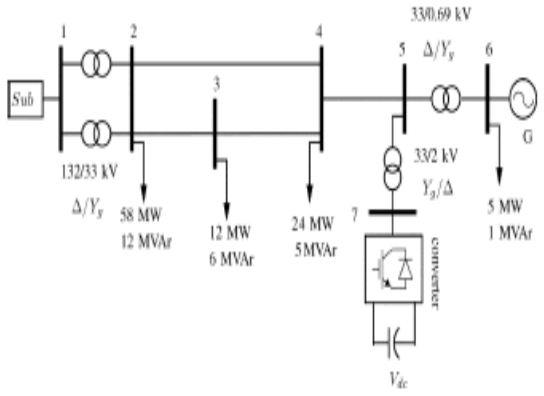
The Voltage controller analyzed in this section and its block diagram exhibited in figure 4. Such controller consist of a phase locked loop (PLL) which synchronize the output three phase voltage of the converter with the zero crossing of the fundamental component of the phase –A voltage . Therefore the PLL provides the Φ angle to abc –dq0 (dq0-abc) transformation .There are four proportional integral PI regulations. One is responsible for controlling the terminal voltage through the reactive power exchange with the ac network. This proportional integral regulator provide the reactive current reference Iq* with the limited between +1 p.u. inductive. This proportional integral regulator has one droop characteristic usually ±5%, which allows the terminal voltage varies a small amount to avoid oscillations. Second proportional regulator is responsible to keep constant the dc voltage through small active power exchange with ac network. This proportional integral regulator provide Id reference value. The other two proportional integral regulators determine Vd and Vq reference voltage components which are sent to the PWM signal generator of the converter, after a drop- to- abc transformation. Finally Vabc are the three phase voltages desired at the converter output.



DSTATCOM Voltage Controller

V. DISTRIBUTION SYSTEM MODEL - I

For this analysis all circuit components were represented by presented by three-phase model, constant current model is active component of loads and constant impedance model is reactive components. The Distribution feeders were modeled as series RL Impedances. The loads are simulated using three parallels RL impedances wye-connected, with the neutral connected to the ground. The three phase transformers are simulated taking into account the core losses. Which is a 132 KV , 60 Hz, sub transmission system with a short circuit level of 1500 MVA , Represented by a Thevenin's equivalent (sub) which feeds a 33KV distribution system through two 132/33 KV Δ/Y g transformers. An AC generator with a capacity of 30 MW is connected to the network through a 33/0.69 KV transformer. This machine can represent one generator in a thermal generation plant as well as an equivalent of various generators in a small hydro generation and wind plant. Some times these machines were simulated as an induction generator. In this network a Distribution static synchronous compensation with a capacity of 5MVAr connected at bus 5 through a 33/2 KV Δ/Y g transformer. The induction generator and DSTATCOM models are presented in following section.



Source (sub): 132 KV; Zeq=0.00667pu,

Line Parameters

Branch 2-4 , R(pu)= 0.2146 X(pu) = 0.3429

Branch 2-3 , R(pu)= 0.0446 X(pu) = 0.1917

Branch 3-4 , R(pu)= 0.2390 X(pu) = 0.4163

Branch 4-5 , R(pu)= 0.5377 X(pu) = 0.9367

Transformers Parameters

Branch 1-2 , S= 100MVA , R1=R2 (pu)= 4.97×10^{-3}

L1=L2(pu)= 2.77×10^{-3} , Rm=Xm (pu)= 500

Branch 1-2 , S= 100MVA , R1=R2 (pu)= 4.60×10^{-3}

L1=L2(pu)= 2.88×10^{-3}, Rm=Xm (pu)= 500

Branch 5-6, S= 30.5MVA , R1=R2 (pu)= 5.00×10^{-3}

L1=L2(pu)= 2.65×10^{-3}, Rm=Xm (pu)= 100

Branch 6-7, S= 5.0MVA , R1=R2 (pu)= 5.00×10^{-3}

L1=L2(pu)= 2.65×10^{-3}, Rm=Xm (pu)= 100

Load Parameters

Bus =2 ; Vn (KV)=33.0, P (MW)= 58.0, Q(MVA)= 12.0

Bus =3 ; Vn (KV)=33.0, P (MW)= 6.0, Q(MVA)= 12.0

Bus =4 ; Vn (KV)=33.0, P (MW)= 24.0, Q(MVA)= 12.0

Bus =6 ; Vn (KV)=0.69, P (MW)= 0.50, Q(MVA)= 0.1

Induction Generator Parameters

Voltage (V)=690

Power (MVA)=30

H(s)= 1.5

Rs (pu)=0.01

Rr (pu)=0.014

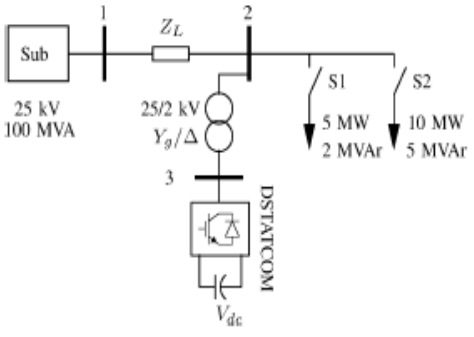
Xs(pu)=0.01

Xr(pu)=0.098

Xm(pu)=3.5

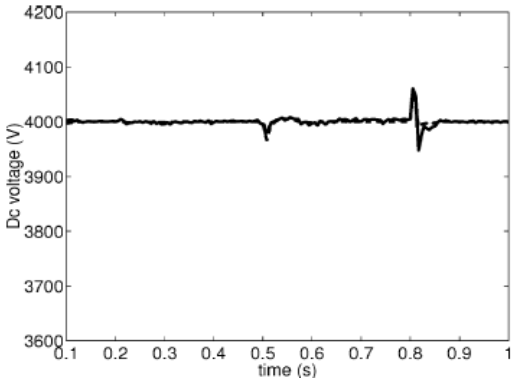
VI. DISTRIBUTION SYSTEM MODEL - II

For this analysis all circuit components were represented by presented by three-phase model, The test system is shown in Fig. system is a 25-kV, 100-MVA, 60-Hz substation, represented by a Thévenin equivalent, feeding a distribution network where there is a DSTATCOM connected at bus 2 through a 25/2-kV transformer. The compensation capacity of the DSTATCOM is MVAr and the voltage level of the dc capacitor is 4 kV.



VII. ANALYSIS

To verify the performance of the DSTATCOM we use here Model -II, in this model a variable load is connected at bus 2 and the substation voltage is also changed during the simulation. The sequence of events simulated is explained as follows. Initially, there is no load connected at bus 2; at ms, the switch S1 is closed and at ms, the switch S2 is closed too; both switches remain closed until the end of the simulation. During these events, the terminal voltage of bus 2 decreases. At ms, the substation voltage is increased to 30 kV, consequently, the terminal voltage of bus 2 also rises.



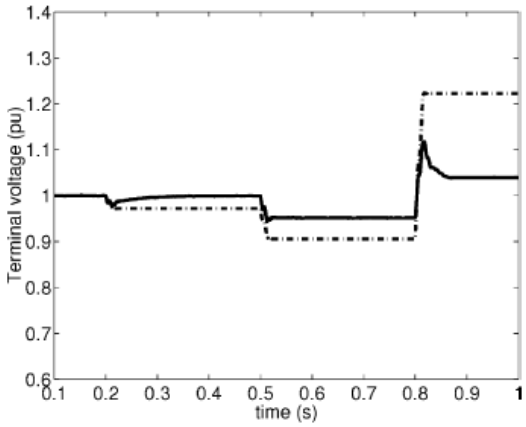
DC voltage of DSTATCOM

The three-phase rms value of the terminal voltage of bus 2 for the events previously described is shown in Fig. In the absence of the DSTATCOM, the terminal voltage varies considerably, but such variations are minimized in the presence of the DSTATCOM.

However, the objective here is to show that the results obtained using the detailed and simplified models are very similar. where the consumption of active or reactive power by the DSTATCOM is represented by positive values and the generation by negative values. Practically, there is no difference among the results obtained from the simplified or detailed models and, therefore, the simplified model can represent very well the dynamic behavior of the DSTATCOM.

In the detailed model case, the switching instant is determined by using interpolation. Thus, even if the switching instant occurs between two integration steps, it is accurately simulated. However, the integration step size should be chosen small enough to avoid that various switching occur between two integration steps. As the switching rate utilized for the PWM was 3000 Hz, considering a 60-Hz system, one switching may occur at each 5.556 s (1/60/3000 s). Thus, the detailed model requires an integration step of 5.556 s to show suitable accuracy. On the other hand, the integration step adopted for the simplified model was 50 times larger (i.e., 277.78 s (50/60/3000 s). Consequently, it is theoretically possible to obtain a speedup of 50 times.

In this section, the simplified model is validated and the simulation results are presented. In the absence of the DSTATCOM terminal voltage varies. In the case Simulated without a DTATCOM all reactive power demand of the induction generator is provided from a three phase capacitor bank; the terminal voltage is equal to 1 P.U. during steady state. In this section, the simplified model is validated, comparing it with the detailed model by using EM transient simulations.



Terminal Voltage of the Bus

VIII. CONCLUSIONS

This analysis shows that the study about the behavior of a DSTATCOM to improve the voltage stability of distribution networks with induction generators. A simulation result shows that such devices can increase the voltage stability limit. Moreover, it can be verified that when the DSTATCOM is controlled by voltage its impact on stability is more effective tan the control by power factor.

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PSoC Driven Myoelectric Hand Controlled using Simulink EMG Pattern Recognition Model

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Abstract **-** Intelligent manipulation and grasping capabilities of a human hand has always been a very challenging and interesting research topic. This paper proposes the control of a myoelectric hand by analyzing and classifying electromyogram (EMG) signals. The surface EMG signal sensed is imported into a standalone host computer through data acquisition card at the rate of 2000 samples per second. The EMG pattern signatures are extracted for each movement followed by training the neural network. The output from the classifier triggers the Integrated Development Environment of the microcontroller which actuates the servo to perform various movements like gripping. The mechanical design of the prototype is compact with two degree of freedom that has the potential to improve the functionality of any prosthetic hand by creating an orientation that more closely matches the grip requirements. The prototype of myoelectric hand described in this paper can be utilized for applications requiring low weight, compactness, less trauma and fast responsive system.

Keywords **-** *myoelectric, microcontroller, feature extraction, pattern recognition, gripping.*

I. INTRODUCTION

Human hands are capable of many dexterous grasping and manipulation tasks with just an impulse from our senses. It would impose a herculean task to replicate this nature's wonder on machines. Recent technological developments has given cheaper and lighter motors, smaller and more powerful microcontrollers enabling better solutions. Most of the existing and emerging robotic hands are developed as prosthetic devices, and hence, our focus has been on making them lightweight, easy to power and operate. The control is based on the fact that amputees still have the phantom of functions and hence are able to generate a repeatable (although gradually varying) EMG signals[1][3].

II. MATERIALS AND METHODS

EMG signals are electrical manifestation of neuromuscular activity associated with contracting muscles. The signals generally are in the range of 10-2000Hz and 10μV-50mV. Usually the usable signal energy is in the 10-500Hz zone [4]. EMG signals acquired from the surface of the skin using disposable pre-gelled surface electrodes for two different hand movements namely finger flexion and wrist up are passed through the precision instrumentation amplifier and the band pass filter. In EMG-based pattern recognition system, sEMG (surface EMG) signals are first preprocessed, and then some features are extracted before performing classification. Normally preprocessing and signal conditioning are performed to suppress noise and improves spectral components of the signal. Various time-domain features extracted from these signals are then passed to the neural network (NN) block for classification. The output of the NN block is used to drive the motor through the microcontroller.

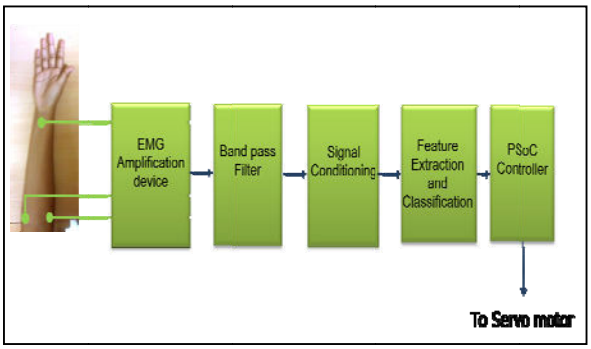

Fig. 1 : Block diagram of the proposed system

III. ACQUISITION SYSTEM

The signals picked up by the electrodes are amplified using AD624AD, a high precision instrumentation amplifier with a gain of 1000. The amplified signals were passed through a band-pass filter implemented using a high pass filter with a cut-off frequency of 50Hz followed by a low pass filter with 500Hz cut-off frequency. The output from the bandpass

filter stage is shown in Figure 2. The filtered signal is imported into a standalone host computer through NI USB 6009 for processing in MATLAB. The NI Data Acquisition (DAQ) card is configured to read the input at 2000 samples per second via the analog input terminal AI0.

IV. SIGNAL PROCESSING AND PATTERN RECOGNITION SYSTEM

The signals obtained were dominated by 50Hz power line interference which was removed using Adaptive filters implementing LMS algorithm.

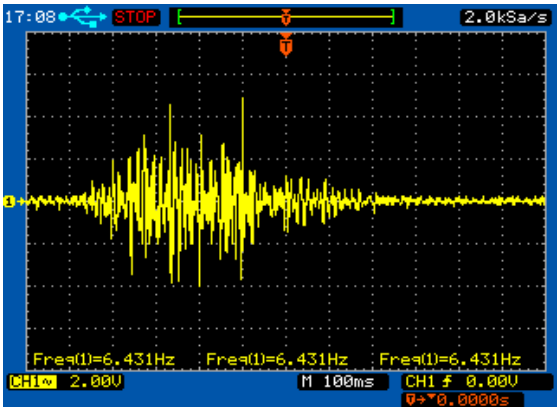

Fig. 2 : EMG signal acquired for male subject during contraction at 2000 samples per second

A filter length of 15 and a step size (mu) of .005 were chosen and an appreciable reduction in the power line interference was observed. The signal is windowed into 7 segments containing 600 sample points per segment with an overlap of 300 sample points. The various time-domain features extracted from the acquired signal includes Integrated EMG (IEMG), Mean Absolute Value (MAV), Modified Mean Absolute Value 1 (MMAV1), Modified Mean Absolute Value 2 (MMAV2), Simple Square Integral (SSI), Variance, Root Mean Square (RMS), Waveform Length (WL), Zero Crossing (ZC), Slope Sign Change (SSC), Difference Amplitude (DA), Willison Amplitude (WA) and Histogram of EMG.

Figure 4: Simulink block for serial communication

These time domain features are most popularly used in EMG pattern recognition system for their computational simplicity. These features were extracted from each segment and the mean of these segments was given as input for training and testing the neural network. The simulink block of the signal processing and pattern recognition system is shown in Figure 3. The communication between the simulink MATLAB and PSoC is achieved through serial communication using the block shown in Figure 4.

A dataset was created from 30 male subjects constituting to about 150 samples with 75 samples for finger flexion and another 75 for wrist up movement. The data are classified by using feed forward back propagation neural network based on the scaled conjugate gradient algorithm. The input is fed into the neural network by dividing into three groups: 70% for training, 15% for validation and 15% for testing. An accuracy of 78.8% for training, 87% for validation and 82.6% for testing was obtained. This constituted to an overall accuracy of 80.7%.

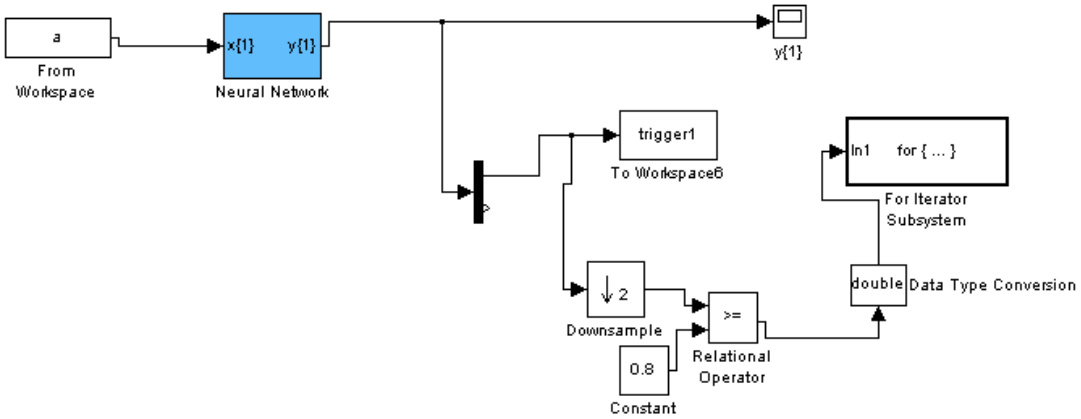

Fig. 3 : Simulink block of pattern recognition stage

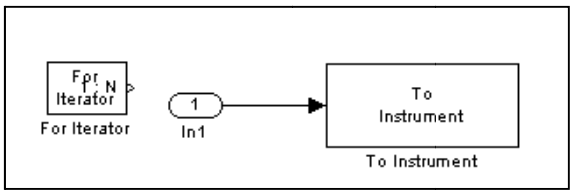

Fig. 4: Simulink block for serial communication

V. PSoC MICROCONTROLLER

The control system of the myoelectric hand is constructed using the Programmable System on a Chip (PSoC) controller which is a family of integrated circuits made by Cypress Semiconductors. PSoC is a true programmable embedded system integrating configurable analog and digital peripheral functions, memory and a controller on a single chip. The control signal for the hand movement is programmed on CY8C29466 chip. The major user modules required to realize the control signals for the motor include Universal Asynchronous Receiver Transmitter (UART) and Timers. The internal clock of the controller is set at 24MHz. In addition PSoC has an internal frequency pre-scaler VC1, VC2 and VC3.

A. UART Module

The binary output from the neural network block is received by the PSoC controller via UART. This supports duplex RS-232-compliant, data format serial communications over two wires. Received and transmitted data format includes a start bit, optional parity and a stop bit. The port pin for receiving the serial data is set to Port 0 pin 7. The UART buffer size is set as 8 and the interrupt mode for transmission occurs every time the transmission register becomes empty. VC3 generates the baud clock for the UART by dividing 24 MHz by 156. The UART internally divides VC3 by 8, resulting in a baud rate of 19,200 bps. The other parameters of the UART block are set to default.

B. Timer Module

For controlling the angle and speed for the servo motor a pulse of variable is required. Here two 8 bit timers are used for clockwise and anticlockwise turns. The PSoC 8 bit timer provides down counters with programmable period and capture ability. The control register is used to start and stop the timer. Once started, the timer operates continuously and automatically reloads its internal value from the period register upon reaching terminal count. The clock frequency of the timer is set as 100kHz. The compare type and interrupt type are configured as less than or equal and compare true respectively. Timers with higher resolutions like 16 bit or 32 bit could also be chosen to achieve precise step movement in the motor. The pulse width of each pulse train is determined by the loaded count value. The user module blocks and the interconnections used are shown in Figure 5.

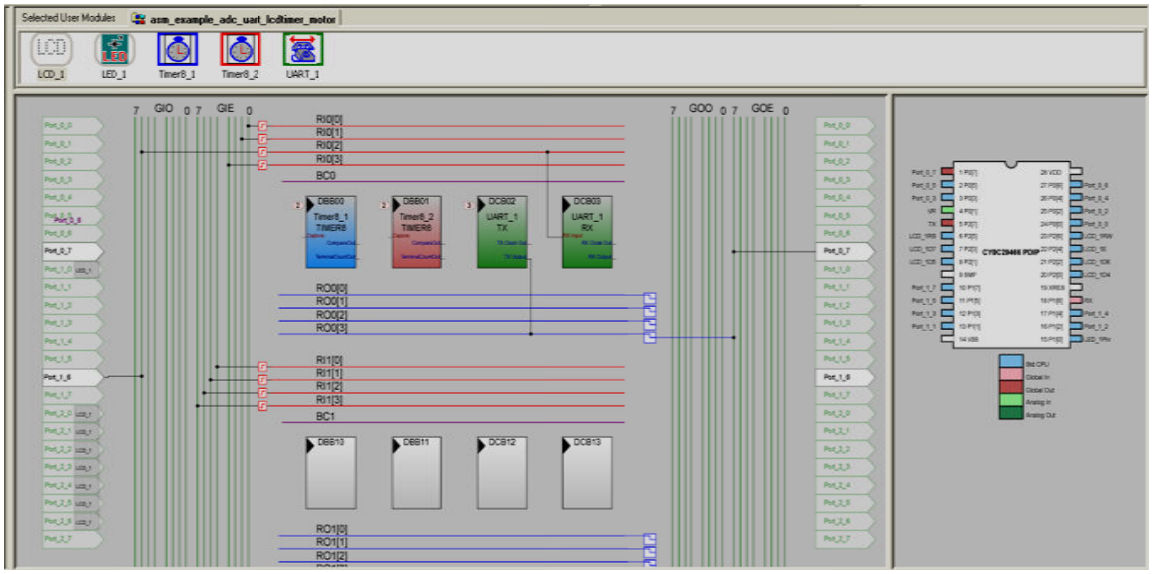

Fig. 5: Application Editor Window of PSoC IDE showing the user modules and interconnections

The period count could be calculated from

$$\frac{\text{Pulse Width (ms)}}{\frac{1}{\text{System clock frequency}} * VC1 * VC2} - 1 = \text{Count}$$

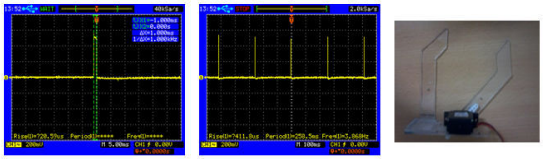

Fig. 6 : 1.05ms Pulse Width to turn the servo motor in clockwise direction

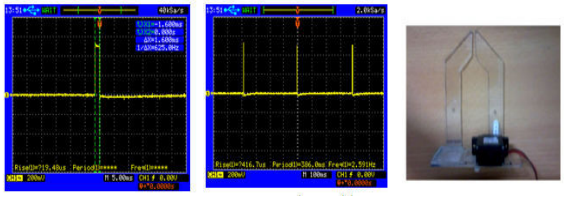

Fig. 7: 1.5ms Pulse Width to bring the servo motor to its neutral position

The neutral position of the servo lies at 1.5ms. A pulse train of 1.05ms can actuate the motor in the clockwise direction for opening the first finger, shown in Figure 6 and 1.5ms gives an anticlockwise turn for closing as shown in Figure 7. Each pulse actuates the motor for an angle of 22º. Thus a series of pulses repeated for every 20ms were transmitted for making continuous movement of the finger element.

VI. MECHANICAL DESIGN OF THE HAND PROTOTYPE

The photograph of the hand prototype shown in the Figure 4 is a gear controlled two fingered prosthesis with a fixed thumb and a movable first finger. To make the prosthesis light in weight acrylic plastic material is used in fabrication. The first finger has one degree of freedom actuated by a servo motor Vigor VTS 05A. It features high capacity, high current wire for low resistance while maintaining standard servo dimensions of 22mm x 13mm x 24mm and weighs about only 8g. The operating speed is $0.17\text{sec}/60^0$ at 4.8 V and has a stall torque of 1 kg/cm.

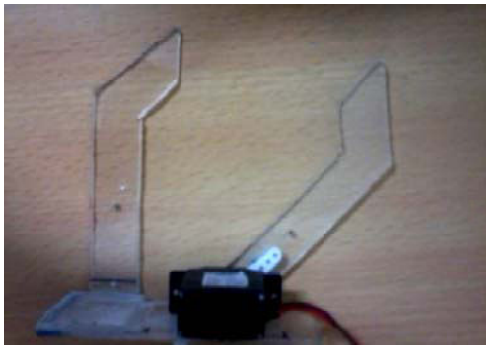

Fig. 8: Prosthetic hand prototype with a movable first finger

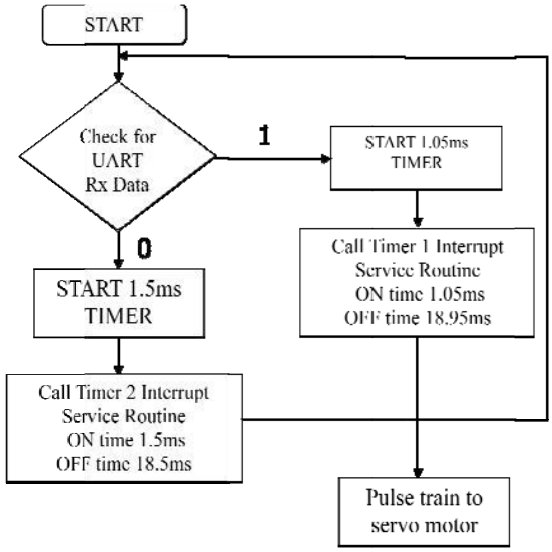

Fig. 9: Flowchart of the Servo motor control using PSoC microcontroller

For the motor control the important parameters to consider are minimum pulse, maximum pulse and repetition rate which is set by the timers of PSoC controller. The pattern recognition system is integrated with the hand module where the motor is controlled to manipulate the prosthetic hand to perform the required gripping action when demanded.

VII. RESULTS AND OBSERVATION

The EMG signals sensed from the subject's forearm muscles Flexor Carpi Ulnaris (FCU), Extensor Carpi Radialis (ECR) and Extensor Digitorum (ED) were found to be sufficient to classify wrist contraction and wrist up movements. The classification accuracy was found to be 80.7%. The complete setup of the Myoelectic hand using PSoC microcontroller is shown in Figure 9.

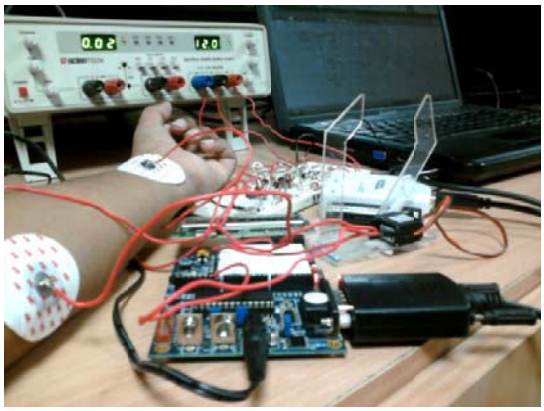

Fig. 9 : The complete setup of the prosthetic system.

Proper shielding of the acquisition system would give more accurate data immune of the ambient noise. The binary output from the neural network is transmitted to the microcontroller via RS232. The microcontroller is programmed to generate the Pulse Width Modulation signals required for actuating the motors which in turn bring about the desires movement in the prosthetic hand.

VIII. CONCLUSION

We proposed a two fingered gear driven prototype for grasping action controlled by the EMG pattern recognition system. This system has more advantage of being low-power, versatile, light-weight and compatible than the currently available prosthesis. The design of the current prototype can be easily altered to house more digits with increased degrees of freedom to bring about pronation and supination of the wrist in addition to the flexion and extension motions. Further work is recommended to design a more sophisticated prosthesis with an addition of more motors to form a dexterous prosthetic hand.

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Analysis of Normal and Pathological Voices Based on Nonlinear Dynamics

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Abstract **-** This paper presents an analysis system aiming at discriminating between normal and pathological voices. Traditional linear methods have several limitations for distinguishing these classes. Hence, this paper illustrates the necessity of moving from the paradigm of linear methods to nonlinear methods for analysis purpose. The measures that are discussed include discrimination by the estimates of nonlinear chaotic-based measures like phase plane plots, estimating the Lyapunov exponent from the trajectory set along with computation of the Shannon entropy and the permutation entropy. These measures were obtained by processing the speech signal directly than using the traditional method of analyzing the glottal flow waveform for assessment. The significance of the work lies in the *noninvasive* approach to analysis and the feasibility to work with low cost computer machines.

Keywords- *Noninvasive; pathological; nonlinearity; chaotic; phase-plane; entropy.*

I. INTRODUCTION

Identification of vocal fold pathologies is a task that is undertaken since 1950's. It is an analysis that requires considerable amount of investigation due to the diversity in the different types of speech pathologies that exist [1], [2]. The presence of vocal fold pathology can cause significant changes in the vibratory patterns of vocal folds. Therefore, it has an impact on the resulting quality of speech production. The *voice quality* depends on the level and extent of glottal opening or closing. Certain laryngeal pathologies prevent the vocal fold from *complete* closure during glottal vibration. Incomplete glottal closure can happen due to the following:

- Paralysis or injury to one or both vocal folds,
- Asymmetry in vocal folds due to irregular growths,
- Swelling of the vocal folds,
- Different muscle tension or length of the vocal folds.

Figure 1a depicts the case of normal vocal folds. It can be seen that vocal folds are smooth with no irregular structure on the surface of the vocal folds, while in case of disease related to the larynx (as shown in figure 1b), the discontinuity on the edges prevent smooth closure of the vocal folds during vibration. There are techniques available in the medical field for detecting the pathologies. However, these methods require direct inspection of the vocal folds (e.g., laryngoscopy, videoscopy, etc.). As a result of which the cost and time of diagnosis using such clinical assessment tools increases.

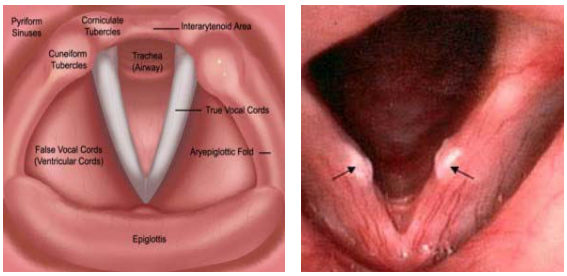


Fig. 1 : A view of the normal vocal folds (After [3]) (a) normal vocal folds (b) pathological vocal folds (After [4]).

A problem to be solved by the noninvasive methods is to predict pathologies in the vocal apparatus based on mathematical model of the larynx [9]. Much of the work done in this area is based on the use of acoustic parameters such as amplitude and frequency perturbations (such as shimmer and jitter), noise parameters and also Mel-frequency cepstral coefficients (MFCC) [10]. It has also been reported in [16] that, pitch perturbation computed by measuring difference between durations of adjacent fundamental periods from the recorded acoustical waveforms were able to classify the normal and pathological classes of voices. Since the fundamental periodicity of the speech is established by the activity of the larynx, the most direct approach reported by the study was to investigate if pitch perturbations are due to *irregularities* in the vibration of the vocal folds. Therefore, the magnitude of perturbation

factor may serve to detect certain types of pathological condition.

Apart from pitch variations, in [17] an analysis system using information only from the correlation between acoustic descriptors in order to discriminate the normal and pathological class is introduced. The correlation of the signal with itself is used to check the self-similarity among the samples. It describes the *temporal* and *spectral* features that can be extracted for classification and then the correlation between features is computed. In [17], correct classification of 94.7 % for pathological and 89.5 % for normal voices is reported. However, it has been studied that the speech production mechanism cannot be analyzed only by the above mentioned measures. The several factors that contribute to the nonlinear measures include the nonlinear pressure at the glottis, nonlinear stress strain of the vocal fold tissues and the nonlinearities with the focal fold collision.

In a qualitative classification of vowels [11], the authors reported three classes of sounds, *viz.,* periodic, aperiodic and irregular. Normal voices fall into periodic or aperiodic. In voice pathologies, because of imbalance of tension between the left and the right vocal folds, the natural vibratory frequencies of two vocal folds ones are quite different. In this case, vocal fold's oscillations are *aperiodic* and *irregular* but in addition some of the signals do fall in the category of periodic signals and therefore create problem in classification. Therefore, the authors are more inclined to use nonlinear time series analysis to estimate the disordered speech. Moreover, their behaviors are in a chaotic manner.

During 1990's, a pioneer work in nonlinear speech processing was done by Kumar and Mullick [6]. They applied nonlinear dynamic analysis into speech time series of normal voices. Zhang *et. al.* [21] studied the efficiency of nonlinear dynamic measures, such as phase space reconstruction and correlation dimension, in comparison with acoustic perturbation measures, to analyze sustained vowels which were pronounced by normal subjects and the patients with unilateral laryngeal paralysis. In the analysis of nonlinear behavior the embedding attractor reconstruction is the starting point. The phase plane plot is the base to classify the two classes. This reconstructed attractor contributes to the phase plane domain. The aim is to analyze the role of the divergence of trajectories in differentiating between the two categories. In addition to the features based on the phase plane domain, literature also involves work in the context of information theory [9], [11], [15]. The effectiveness of entropy to evaluate the randomness is illustrated to quantify the difference between the normal and the pathological voice. These techniques are essential to characterize the speech signals and results obtained will lead to a good foundation for development of an automatic system for characterization purpose.

II. METHODS

A. Traditional Acoustic Methods

1. Jitter

In speech processing, jitter of a signal means the cycle to cycle variation in the pitch period [18]. As seen in the Glottal Flow Waveform (GFW) of normal vocal folds shown in figure 2, the three phases repeat itself after certain interval. Each interval is called the *pitch period*. The pitch period is quasi-periodic in case of normal voices while in case of abnormal voices the vocal folds are not closed properly due to abnormal growth of mass on the vocal folds and hence the pitch period may or may not be present. This cycle to cycle variation in the pitch period is known as the *jitter* and is also represented by the *pitch perturbation quotient* (PPQ). It has been estimated that in case of pathological voices the jitter variation is larger than that in the normal speech signal [7].

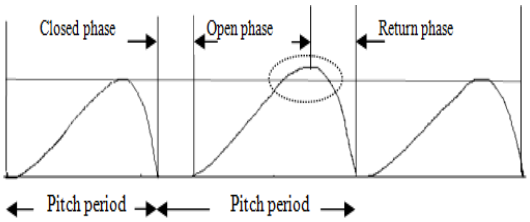


Fig. 2 : Glottal flow waveform

2) Shimmer

The *shimmer* in the signal is the representation of the cycle to cycle variation in the amplitude. As seen in the GFW of the normal vocal fold in the figure 2, the amplitude in the open phase need not be same all the time (as indicated by dotted circle). The difference in the pressure developed at the glottis causes the variation in the air-flow and hence the amplitude in the open phase in the waveform is not constant. The variation in the amplitude of the air flow velocity in each cycle constitutes the shimmer in the signal and is also represented by the *amplitude perturbation quotient* (APQ). It has been validated that shimmer is more in the case of pathological signal as compared to that of the normal speech signal [7].

3) Other Acoustic Measures

These techniques focus on regular time and frequency analysis of voiced speech. The variation of pathological voices is measured during phonation of sustained vowels. In addition, the other methods of screening the laryngeal pathology includes period variability index (PVI), harmonic to noise ratio (HNR), stability of pitch generation (STAB), ratio of energy concentrated in the cepstral pitch impulse to total cepstral energy (PECM), etc [7].

4) Correlation-Based Methods

The correlation coefficient is computed as (for two numeric sequences x and y whose length is N) in [17] as

$$R_{xy} = \frac{\sum_{i=n}^{N}(x_i - \bar{x})\times(y_i - \bar{y})}{\sqrt{\sum_{i=n}^{N}(x_i - \bar{x})^2}\times\sqrt{\sum_{i=n}^{N}(y_i - \bar{y})^2}}. \quad (1)$$

The values of the correlation coefficient are restricted into the interval $[-1,1]$, $|R_{xy}|=1$ corresponding to perfectly correlated sequences and $|R_{xy}|= 0$ to perfectly uncorrelated sequences. The correlation matrix for a normal subject and a pathological sample are presented in figure 3a and 3b, respectively. When looking at those matrices, one can see that their structures are quite different. That is why it was decided to exploit the information from the correlation matrix rather than the features themselves in order to see if significant differences could be found between normal and pathological samples.

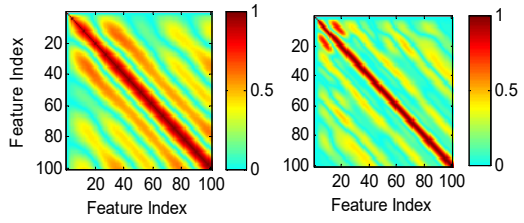


Fig. 3 : (a) Correlation matrix for a normal sample (b) correlation matrix for pathological sample.

The correlation matrix is computed by (1) for the normal sample contains more elements close to 1 (in absolute values) than the one for the pathological sample. Information could be extracted from the correlation matrix by considering the elements of the upper part of this matrix and by considering each of these elements as a *feature* itself. The correlation matrix is symmetric and its diagonal elements are nearly equal to one. Hence, correlation measures can form a useful feature set to classify the normal and the pathological voices.

In spite of good classification rates, the traditional method of jitter and shimmer were not sufficient. Also for these methods, the GFW is used which is not easily obtained as that of speech signal. The analysis by correlation of features was not suitable as it did not exploit the *nonlinearity* in the speech production model. The speech is an outcome of a nonlinear system (i.e., vocal tract and its interaction with the source) and hence should be evaluated on the basis of nonlinear dynamics. As a result, technology paved way from linear methods to those based on information theory, nonlinear dynamics and chaos.

B. Entropy Based Measures

1) Shannon entropy

The entropy of a signal is a measure of the randomness of the signal. It determines the degree of uncertainty and hence information content in a signal. If N is a discrete random variable with set of alphabets χ and having probability mass function $p(x) = \Pr\{X = x\}$, $x \in \chi$. Then the entropy $H(X)$ of a discrete random variable X is defined as [19],

$$H(X) = -\sum_{x_i \in \chi} p(x_i)\log p(x_i). \quad (2)$$

Shannon entropy has been used with several modifications has been used in [12] for classification purpose.

2) Parametric Entropy

The parametric entropy is a complexity measure for time series based on comparison of neighboring values. The advantages of this measure lies in the simplicity and fast calculation. Consider a time series such that $x(t)$, then for all $n!$ permutations π of order n which can be considered here as possible order types of n different numbers. For each π, we determine the relative frequency as [8],

$$p(\pi) = \frac{\#\{t \mid 0 \le t \le T-n, (x_{t+1,\ldots,}x_{t+n})\}}{T-n+1}. \quad (3)$$

The permutation entropy of order $n\geq 2$ is defined in [10] as,

$$H(n) = -\sum p(\pi)\log p(\pi), \quad (4)$$

where the sum is over all $n!$ permutations π of the order n. This is the information contained in comparing n consecutive values of the time series.

C) Phase Space Domain Methods

1. State Space Reconstruction

To study the dynamics of a system it is necessary to construct the attractor. The reconstruction of the dynamical state space from the time series is performed by using the time delay embedding theorem [12]. The state-space is reconstructed by the method of deliberate introduction of delays into the signal. Given a time series $x(n)=\{x_j \mid j=1,2,3.....N\}$ the state space vector formed by the time delayed samples can be expressed as,

$$X_i=(x(i),x(i-\tau),....,x(i-(m-1)\tau)), \qquad (5)$$

where $i=1,2,..,M$, and $M=N-(m-1)\tau$. In (5), m is the embedding dimension and τ is the time delay. Different choices of m and τ yields different reconstructed trajectories. Hence, when determining the phase space their optimum values must be considered. There are different methods to determine an adequate time delay τ. For example,

- Select τ as the first zero of the autocorrelation function [15],
- Select τ as the first local minimum of the average mutual information [15],
- Select τ as the value where the autocorrelation function reaches $1/e$ of its original value for the first time [14].

However, in many cases the value at first local minimum of the mutual information between $x(n)$ and $x(n-\tau)$ is used as τ. The mutual information is given by,

$$I(\tau)=\sum_{n=1}^{N-\tau} p((n),x(n-\tau))\times\log\left[\frac{p(x(n),x(n-\tau))}{p(x(n))p(x(n-\tau))}\right], \qquad (6)$$

where $p(x(n),x(n-\tau))$ gives the joint probability density function (pdf) while $p(x(n))$ and N determines the individual probabilities of the two signals. Therefore, the optimal delay is obtained by minimizing the average mutual information between signal $x(n)$ and $x(n-\tau)$. In the work presented in [15], it has been found that the value of the mutual information at the time of first minimum serves as a feature for classification factor between the two classes. This was because at the time of first minimum, the mutual information in healthy speech samples is more than that of pathological speech samples. The false neighbors method and false strands method can be used to estimate the value of m [13].

To eliminate the use of different methods for calculation of embedding dimension m and time delay τ, we use singular value decomposition (SVD) method to obtain the reconstructed trajectory. For a data series with N number of data points, $x(t)=\{x_j \mid j=1,2,3,...,N\}$. The trajectory matrix X can be constructed from (5) as follows,

$$X=\begin{bmatrix}X_1^T\\X_2^T\\\vdots\\X_M^T\end{bmatrix}=\begin{bmatrix}x_1 & x_2 & \dots & x_m\\x_2 & x_3 & \dots & x_{3m+1}\\\vdots & \vdots & \dots & \vdots\\x_M & x_{M+1} & \dots & x_N\end{bmatrix}, \qquad (7)$$

where $M=N-(m-1)$ and the matrix X is the *pseudo-phase portrait* (by the method of delays) in m-dimensional pseudo- phase space with a delay time of one unit [12]. The SVD of the trajectory matrix in (7) gives,

$$X=S\Sigma C^T, \qquad (8)$$

where, S is the $M\times m$ matrix of eigenvectors of XX^T, C is the $m\times m$ matrix of eigenvectors of X^TX and Σ is the $m\times m$ diagonal matrix consisting of singular values i.e., $(\sigma_1,\sigma_2,...,\sigma_N)$. From the plot of $\log_{10}(\sigma_i/\Sigma_{i=1}^N\sigma_i)$ (as shown in figure 4), i.e., normalized spectra of singular values of the SVD trajectory matrix X, the embedding dimensions can be computed by choosing the index after which the normalized singular values do not have large variation.

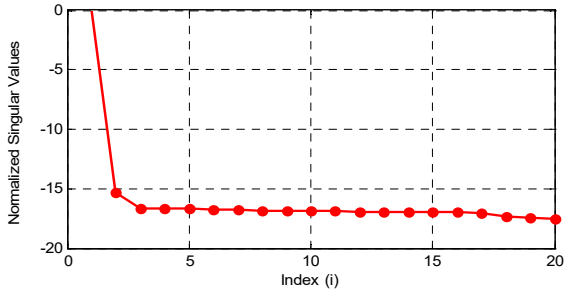


Fig. 4 : Plot for normalized singular values from SVD of trajectory matrix for a normal female voice with N=1000 and sampling frequency 25 kHz.

2) Largest Lyapunov Exponent (LLE)

Lyapunov exponent is efficient in measuring the divergence of initially close trajectories. The chaotic behavior of the dynamical systems is dependent on its initial conditions. Small changes in the initial conditions can bring large changes in the system. This instability is characterized by the Lyapunov exponents, which

quantifies the average exponential rates of convergence or divergence of nearby state space trajectories. The positive and negative exponents imply divergence and convergence, respectively. The existence of a positive Lyapunov exponent for almost all initial conditions in a dynamical system is a common definition of deterministic chaos.

To understand the concept of Lyapunov exponent and to obtain it, consider two close by points on the trajectory x_o and x_o+u_o as shown in figure 5. Here u_o is a small perturbation of the initial point. After a time t the points on the trajectory will be $f^t(x_o)$ and $f^t(x_o+u_o)$ and the perturbation u_t will become,

$$u_t = Du_o, \tag{9}$$

$$f^t(x_o+u_o)-f^t(x_o)=e^{\lambda t}f^t(x_o) \tag{10}$$

$$e^{\lambda t}=\frac{f^t(x_o+u_o)-f^t(x_o)}{f^t(x_o)} \tag{11}$$

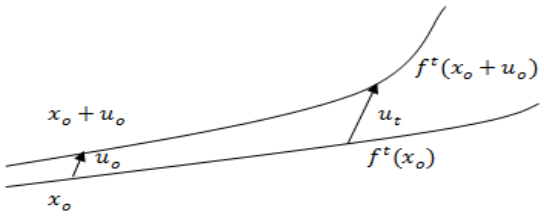


Fig. 5 : Divergence of two nearby trajectories starting from close initial points.

Here the value of λ obtained from (11) is the Lyapunov exponent. A chaotic system will have least one positive Lyapunov exponent. The algorithms for calculating Lyapunov exponents from a time-series were first proposed by Wolf *et al.* [20]. Later on, several algorithms were proposed, but the method presented in [13] is used in this context.

III. EXPERIMENTAL SETUP

A) Data

The experiments for classification are performed on nine voice samples. Three of the signals are normal and remaining are pathological. The six pathological voices are of the following disease of the vocal folds [5]:

- Abductor Spasmodic Dysphonia
- Muscle tension disorder
- Paradoxical vocal fold dysfunction (PVD)
- Dysphonia plica ventricularis (DPV)
- Bilateral vocal fold paralysis
- Presbylaryngis

The sound recordings contain the sustained phonation of the /a/ voice taken from the rainbow passage available freely on [5]. The voice samples are 40 ms in duration and the sampling frequency of each sound is set to 25000 Hz with bit resolution of 16 bits. The speech data is evaluated to get the parameters as discussed in the methods section. The results obtained for each of the speech signal are then showed to understand the variation due the different pathology. The section IV, the first three results are for normal voice signals while the rest corresponds to pathological voice signals.

IV. EXPERIMENTAL RESULTS

For the selected speech samples the results obtained on applying the above discussed methods are evaluated in this section. Entropy has been very essential to note the degree of randomness in the signal. The Shannon entropy has been computed from (2) and shown in the Table I. It can be observed that the values of Shannon entropy are not sufficient to classify all the speech signals effectively.

TABLE I. Results of Shannon Entropy

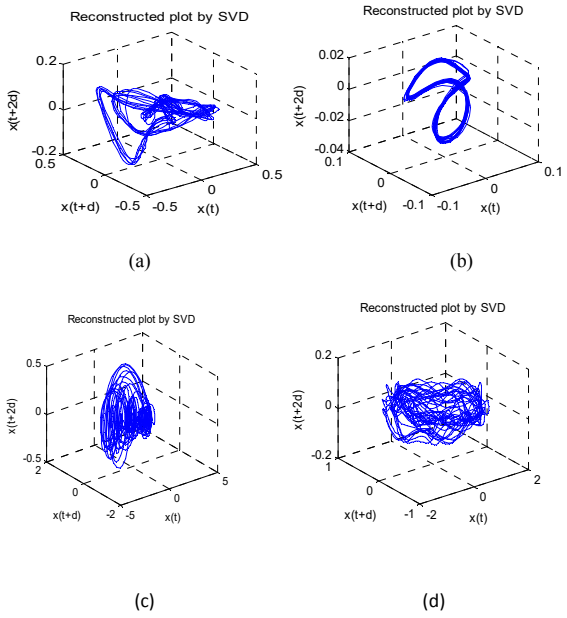
Voices	**Shannon Entropy**
Normal male	4.3828
Normal female 1	4.4635
Normal female 2	4.4260
Abductor SD	4.4187
Muscle tension	4.5088
DPV	3.8100
PVD	4.1234
Bilateral paralysis	4.3613
Presbylaryngis	4.2972

In case of DPV and PVD it is seen that the entropy is much less than that of the normal speech signals. Thereafter, the parametric entropy for the speech signals is computed from (3) and (4) for $n=2$. A variation from low entropy for normal speech signals to higher entropy for pathological voice was observed as in Table II.

Table-II : Results of Parametric Entropy

Voices	Parametric Entropy
Normal male	0.6837
Normal female 1	0.6884
Normal female 2	0.6726
Abductor SD	0.6928
Muscle tension	0.6919
DPV	0.6929
PVD	0.6930
Bilateral paralysis	0.6832
Presbylaryngis	0.6911

Therefore, the entropy of the speech signal will be a useful feature for classification purpose. After analysis of the entropy-based measures, the phase plane plot for the speech signal is constructed by the time delay method as in [11], [15]. Figure 6 shows the phase-plane plots for the normal as well as pathological speech signals. It can be clearly seen that the trajectories are well defined in case of the normal speech signals while in case of pathological speech the trajectories are random. The phase plane plots for Bilateral paralysis and Presbylaryngis were similar to that of the DPV and muscle tension pathology, respectively.



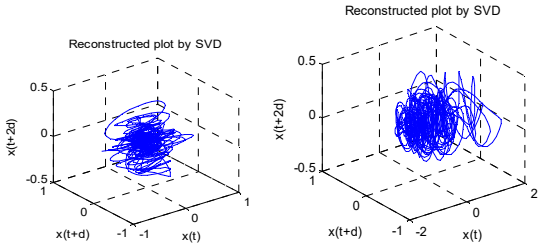


Fig. 6 : 3-D state space reconstructed by the SVD method (a) normal male voice (b) normal female voice (c) Adbuctor sd (d) Muscle tension (e) DPV (f) PVD.

Based on the trajectory matrix that is created for the phase-plane plot, the Lyapunov exponent can also be calculated. The largest Lyapunov exponent is calculated here by the method presented in [14]. The results for the different values of embedding dimension is computed and shown in Table III. The results show that the value of the largest Lyapunov exponent is more for the pathological voice. This is because the divergence of the trajectories in the phase-plane is more in case of the pathological voice, while in case of the normal speech signals the trajectories are well defined and close to each other, therefore the rate of divergence obtained from the exponent is less in comparison to those having unhealthy larynx. Therefore, from the values of the largest Lyapunov exponent it can be stated that the Lyapunov exponent is a very effective parameter for classification purpose.

Table – III : Results of Largest Lyapunav Exponents (LLE) for different values of *m*

Voices	m=1	m=3	m=4	m=5	m=10
Male	0.35	0.19	0.18	0.18	0.09
Normal Female 1	0.29	0.18	0.15	0.13	0.059
Normal Female 2	0.35	0.21	0.18	0.15	0.062
Abductor SD	0.40	0.29	0.21	0.20	0.15
Muscle tension	0.46	0.31	0.27	0.24	0.15
DPV	0.55	0.22	0.17	0.15	0.084
PVD	0.54	0.38	0.34	0.31	0.22
Bilateral paralysis	0.54	0.41	0.37	0.34	0.25
Presbylaryngis	0.42	0.27	0.19	0.13	0.085

The values obtained can also be compared to the phase plane plots. As seen from the plots that the state space plot for female voice is least diverging and the trajectories are most close to each other, as a result the largest Lyapunav exponent is the smallest. While the value of LLE of DPV and PVD is largest as should be from its complex structure in figure 6e and 6f, respectively. The value of the largest Lyapunav exponent can then be used as a feature to perform classification of the normal and pathological voices. The presence of positive value of the exponent is an indication of chaos. However, it can be seen that the sensitive dependence in case of the pathological signal is more than that of the normal speech signal. It is because of this ability the Lyapunov exponent is a state-of-the-art method

V. SUMMARY AND CONCLUSION

In this work, the usefulness of the Shannon entropy, permutation entropy and that of the complexity measures like Lyapunov exponent has been evaluated in order to distinguish between pathological and normal voice. The phase-plane plots instead of being constructed from the traditional delay method are reconstructed by the SVD method. The reason for choosing the SVD method is that it is not only applicable to chaotic time series but also to ordinary deterministic signals. SVD method of reconstruction has an advantage that the embedding dimension can also be obtained from the singular values. In addition, the reconstructed is obtained just by unit delay.

Therefore the analysis done by nonlinear methods can be used further for classification and to develop a system for pathology diagnosis in the speech production system, which is encouraging future research work.

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Feasibility Study of Solar-Wind Hybrid Power System

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Abstract **-** This paper presents feasibility study of hybrid power system. Rapid depletion of fossil fuel resources necessitated research on alternative energy sources. A wind-solar hybrid system is a reliable alternative energy source because it uses solar energy combined with wind energy to create a stand-alone energy source that is both dependable and consistent. Solar power or wind power alone can fluctuate, when used together they provide a reliable source of energy. The perfect solution is to combine these two forms of energy sources to create a constant energy flow. Main objective of this paper is to study feasibility of stand-alone solar-wind hybrid power system and to maximize use of renewable energy generation system while minimizing the total system cost.

Index Terms*—Homer, Hybrid System, Optimization, Solar, Wind*

I. INTRODUCTION

Solar energy and wind energy have been deemed clean, inexhaustible, unlimited, and environmental friendly. Such characteristics have attracted the energy sector to use renewable energy sources on a larger scale. However, all renewable energy sources have drawbacks. Wind and solar sources is dependent on unpredictable factors such as weather and climatic conditions. Due to both sources' complementary nature, some of these problems can be overcome the weaknesses of one with the strengths of the other. This brings us to the hybrid solar-wind power plant concept. Hybrid energy stations have proven to be advantageous for decreasing the depletion rate of fossil fuels, as well as supplying energy to remote rural areas, without harming the environment.

Distributed Generation (DG) refers to small power plants (a few watts upto 1MW) at or near the loads, operating in a stand-alone mode or connected to a grid at the distribution or sub-transmission level, and geographically scattered throughout the service area. Distributed Generation includes small, modular technologies for electricity generation, located close to the load. DG technologies are used both in stand-alone mode as well as in grid parallel mode. Conventional electricity generating stations are typically located close to the fuel source and away from the loads generated is conveyed through the transmission system to the load centre, which often requires large investment. Transmission and distribution costs account for about 30 per cent of the cost of delivered electricity. DG technologies obviate the need for an expensive transmission system and minimize transmission and distribution losses.

The Hybrid Optimization Model for Electric Renewables (HOMER) software is used as a tool to carry out the research. The main objective of this paper is to assess the feasibility and economic viability of utilizing hybrid Solar–Wind–battery based standalone power supply systems to meet the load requirements.

The hybrid of picohydro, PV, wind turbine, generator and battery as back-up is the basis of assessment. The results from the simulation of renewable hybrid system shows that in order to reduce the COE, it is important to look into the amount of excess energy the system produced. COE is defined as the ratio of total annualized cost and annual load served, reducing the annualized or/and increasing the annual load served should be one of the objective of optimization [1].

[2] discusses on the optimization of the renewable energy hybrid system based on the sizing and operational strategy of generating system. In this case study, PV array system, wind turbine, diesel generator with battery and converter are the components chosen for the analysis. HOMER simulates the system based on the estimation of installing cost, replacement cost, operation and maintenance cost, fuel and interest.

[3] will discuss cost benefit analysis of solar-wind hybrid power system at Nigeria done using HOMER software and comparison was also made with the cost per kilowatt of central grid or utility supply. The hybrid

system have a payback period of about 33 years and at current costs, central grid power is the least expensive option but may not be available to most rural households far from the grid. Simulation is done using Homer software and found that wind-solar cell hybrid energy system would be cost effective if there is reduction in component cost by installation of many of this hybrid system in a farm thereby lowering the investment cost per kilowatts.

II. WIND POWER

Wind is a natural phenomenon related to the movement of air masses caused primarily by the differential solar heating of the earth's surface. Seasonal variations in the energy received from the sun affect the strength and direction of the wind.

The wind turbine captures the winds kinetic energy in a rotor consisting of two or more blades mechanically coupled to an electrical generator. The turbine is mounted on a tall tower to enhance the energy capture.

III. SOLAR POWER

The solar modules (photovoltaic cell) generate DC electricity whenever sunlight falls in solar cells. The solar modules should be tilted at an optimum angle for that particular location, face due south, and should not be shaded at any time of the day.

IV. Hybrid Solar-Wind system

A stand-alone wind system with solar photovoltaic system is the best hybrid combination of all renewable energy systems and is suitable for most of the applications, taking care of seasonal changes. They also complement each other during lean periods, for example, additional energy production through wind during monsoon months compensate the less output generated by solar through wind during monsoon months compensate the less output generated by solar. Similarly, during winter when the wind is dull, solar photovoltaic takes over. The hybrid solar wind power system is as shown in figure 1.

Application :

- Remote and rural village electrification
- Ideal for cell phone recipient stations,
- Residential colonies and apartments for general lighting
- Street lighting

With the use of renewable energy based system the emission of carbon and other harmful gases are reduced to approximately 80% to 90% in environments

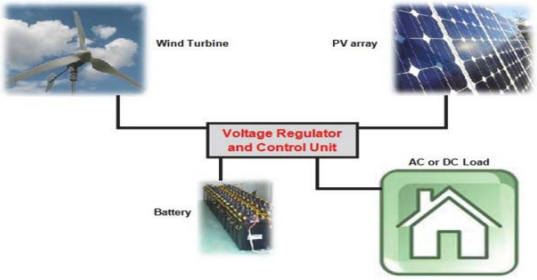

Fig:1 Solar-wind hybrid power system

V. ANALYSIS METHOD

The HOMER is a micro power optimization software developed by Mistaya Engineering, Canada for the National Renewable Energy Laboratory (NREL) USA, which can useful for evaluating designs by simplifying the given task for both off-grid and grid-connected power systems for plenty of applications . It also provides the cost benefit analysis for hybrid energy system. In designing any power system, the decisions about the configuration of this system needs to be analysed, like components and its specification for the system design, size of that all components, the availability of energy resources and technological options, and the cost of each available technology, all these information are difficult to achieve.

HOMER simulations are performed by analyzing energy balance calculations and show the all possible configurations. This all possible configuration arranged by net present cost which can be useful for comparison of system design. HOMER's optimization and sensitivity analysis make this task easier. Also it finds all possible system configurations related to it

Six different locations are selected for analyses i.e. are Vadodara, Ahmedabad, Surat, Mundra Khambhat, Junagadh. Solar radiation data for tilted panel and average wind speed data at 50 m above the surface of the earth is taken from NASA website[6]. HOMER consider all cost in dollars, so conversion we take for this simulation is 1$= 50 INR.

VI. SIMULATION

We consider six different locations i.e. Surat, Vadodara, Ahmedabad, Khambhat, Mundra, Junagadh and two load condition i.e. 5KWh/day and 10 KWh/day for simulation.

Components to be considered for standalone solar-wind hybrid power system.

Wind turbine :

Type: Air Stream 1 KW

Rated power: 1 KW DC

Life time: 15years

Hub Height: 25m

PV panel:

Rated power : 1KW DC

Slope: 30

Lifetime: 20years

Battery:

Type:Vision 6FM 200D

Nominal Capacity: 200Ah

Nominal Voltage: 12V

Primary load

Type: AC

Rating: 5 KWh/day and 10 KWh/day

TABLE I : COST TABLE

Component	Rating	Cost(INR)
PV panel	1KW	175000
Wind Turine	1KW	113500
Converter	2KW	55500
Battery	12V, 200Ah	10000

VII. ANALYSIS OF RESULTS

The below table shows the summary of result for 5 KWh/day and 10KWh/day for six location.

TABLE II : RESULT FOR 5 KWH/DAY

5 KWh/day						
	Vadodara	Ahmedabad	Surat	Khambhat	Mundra	Junagadh
Initial Capital(INR)	664000	664000	839000	664000	664000	839000
Operating Cost(INR/year)	36250	36250	38600	36250	36250	38600
Total NPC(INR)	1127200	1127200	1332550	1127200	1127200	1332550
Cost of energy(INR/KWh)	48	48	57	48	48	57

TABLE III : RESULT FOR 10 KWH/DAY

10 kWh/day						
	Vadodara	Ahmedabad	Surat	Khambhat	Mundra	Junagadh
Initial Capital(INR)	1041750	980250	1041750	1041750	1041750	1041750
Operating Cost(INR/year)	41950	47600	41950	41950	41950	41950
Total NPC(INR)	1578300	1588900	1578300	1578300	1578300	1578300
Cost of energy(INR/KWh)	33	34	33	33	33	33

The above mentioned results declair that the proposed stand-alone hybrid system will be able to feed the power to the ac load of rating 5 KWh/day and 10 KWh/day, constantly throughout the year.The proposed system is best suitable for ac load. The sensitivity variables considered for the proposed system analysis of stand-alone hybrid system are wind speed, solar insolation and loading condition. The simulation results are evaluated for each one of this sensitivity. An hourly time series simulation for every possible configuration system is achieved for the 1-year period. From all suggested configuration, the best optimal system is kept, which fulfils the condition of meeting the load demand.

VIII. OPTIMIZATION RESULT

After analyzing the simulation, one can suggest that the for higher loading stand-alone solar-wind hybrid system is most suitable, for supplying the power to the ac load. The simulation result suggests that this hybrid system is most suitable for all location. Result suggests that from the different possible configuration, one can choose the better optimal solution. From the optimization results the most suited optimal configuration of energy system components are Airstream 1 KW wind turbine, 1 KW PV-Array. From the result, the total net present cost (NPC), Initial cost, operating cost and cost of energy (COE) for such a system is 1578300 INR, 1041750 INR, 41950 INR and 33 INR/kWh, respectively for one year as shown in table III. This is optimized result for 10 KWh/day.

IX. SIMULATION RESULTS

The simulation result allows only feasible solution with their increasing in number of cost and eliminates all other infeasible possible solutions. Also simulation performs the number of parameters displayed against sensitivity variables to identify optimal solution for energy system. According to the optimal solution the total energy required to satisfy the laod demand by the hybrid combination of 36% PV, 64%wind as shown in figure 2.1 with excess electricity of 35%.

Figure 2.2 shows monthly average electric production from wind energy and solar energy in graph format. Yellow colour indicates electric energy production from solar energy and green colour indicates electric energy production from wind energy.

Production	kWh/yr	%
PV array	2,526	36
Wind turbines	4,536	64
Total	7,063	100

Consumption	kWh/yr	%
AC primary load	3,650	100
Total	3,650	100

Quantity	kWh/yr	%
Excess electricity	2,473	35.0
Unmet electric load	0.0000124	0.0
Capacity shortage	0.00	0.0

Quantity	Value
Renewable fraction	1.00

Fig. 2.1 Optimized result for hybrid solar-wind power system

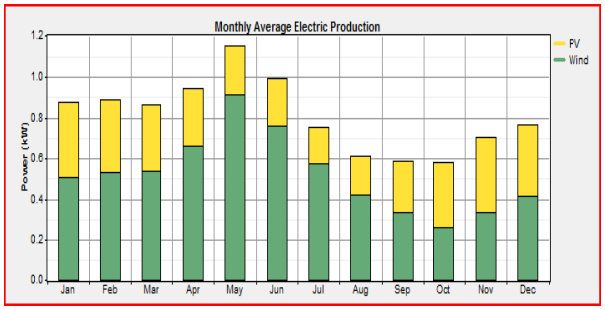

Fig. 2.2 Graphical representation of result for hybrid solar-wind power system

IX. CONCLUSION

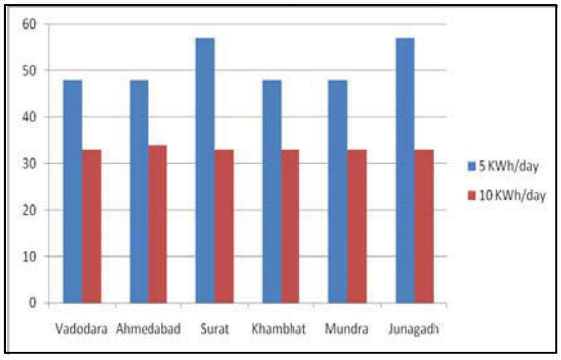

Fig. 3 Graph of location versus cost of energy.

With the help of simulation, the cost of energy production is calculated for Ahmedabad, Vadodara, Surat, Mundra, Khambhat, Junagadh. It can be concluded that for loading condition of 5 units per day the cost of energy production is 48 INR per unit, where for the load of 10 unit per day, the cost of energy production reduces to 33 INR per unit. So it is proved that as loading condition increases per day, the cost per unit will reduce as show in figure 3.

As shown in above figure for 5 KWh/day cost of energy for six selected location is vary in large range but for 10 KWh/day cost of energy is almost constant i.e. 33 rupees per KWh.

Although initial cost for solar-wind hybrid power system is high, but it produces electricity at least cost. Due to distributed generation it eliminates installation cost transmission lines. It has many advantages that it produces no pollution and requires less maintenance. HOMER software is used for the optimization of hybrid combination and gives best combination according to least price. It is feasible to use solar wind hybrid power system for higher loading.

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Design of a Run Length Encoder IP Core

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Abstract - We present a new binary entropy coder for data compression. This new encoder can be implemented efficiently in practice .This encoding can be found in numerous application such as data transfer or image storing. It is a well known, easy and efficient compression method based on the assumption of long data sequences without the change of content. These sequences can be described by their position and length of appearance. This paper describes an algorithm, performing run length compression in hardware.

Keywords-*FPGA, RLE, data compression, compression ratio.IP Core*

I. INTRODUCTION

Run-length encoding (RLE) is a very simple form of data compression in which *runs* of data (that is, sequences in which the same data value occurs in many consecutive data elements) are stored as a single data value and count, rather than as the original run. This is most useful on data that contains many such runs: for example, simple graphic images such as icons, line drawings, and animations. It is not useful with files that don't have many runs as it could greatly increase the file size. Verilog HDL is used to develop the hardware**.**

Data which is compressed using RLE method falls into two categories:

Repeated symbols: This subset of data consists of the symbols that can be compressed by repla- cing them with a number indicating how many times the symbol is repeated and the repeated symbol.

Non-repeated symbols: This subset of data con- sists of the symbols that cannot be compressed because they are not repeated and cannot be predicted. This is the non compressed data.

II. RLE ENCODER

Block diagram:

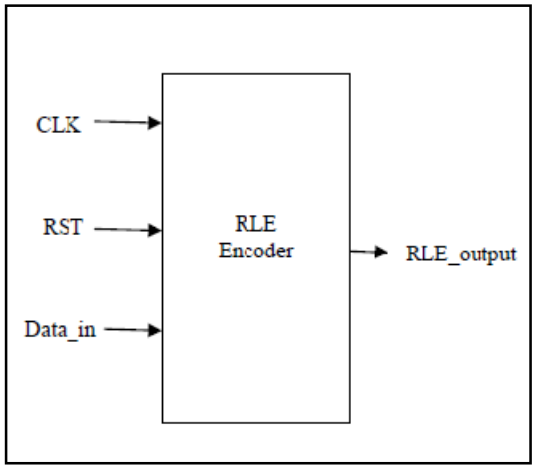


Figure: 1

Block diagram description:

A block diagram of the ports of the run length encoder is shown in Figure 1.This block have 3 inputs clk, reset, data in, encoder data in(5-bit) and one output RLE output(11- bit).The working of encoder is explained below.

Run Length Encoding

Data compression is also called as source coding. It is the process of encoding information using fewer bits than an uncoded representation is also making a use of specific encoding schemes. Compression is a technology for reducing the quantity of data used to represent any content without excessively reducing the quality of the

picture. It also reduces the number of bits required to store and/or transmit digital media.

It is a technique that makes storing easier for large amount of data. It involves transforming data of a given format, called source message, to data of a smaller sized format, called codeword.

Each sequence of information to be coded will contain a set of characters .By run length method of compression, the compressed sequence will have amplitude value as well as the frequency which denotes the number of occurance in the order by which each character value followed by the number of occurance or frequency.

The amplitude by which the character is determined called RUN and the frequency of the character called LENGTH. Thus came the name RUN LENGTH encoding.

So for implementing the run length encoder we need a logic which can identify each character in the input string and could be able to check the number of occurrences of each character. Thus delivering the output in such a way that it shows each character followed by its occurrences as shown in the numerical example below.

In our venture we have hard coded a 64 location array with first location loaded with character 'a' denoted by a 5 bit binary value '00001',second with 'b' denoted by '00010', third and forth with 'd' denoted by '00100' and all the other 60 location with 'c' denoted by '00011'.So a total of 320(64*5) bit input string.

a	**b**	**d**	**d**	**c**	**c**	**c**	**c**
c	c	c	c	c	c	c	c
c	c	c	c	c	c	c	c
c	c	c	c	c	c	c	c
c	c	c	c	c	c	c	c
c	c	c	c	c	c	c	c
c	c	c	c	c	c	c	c
c	c	c	c	c	c	c	c

Fig: input matrix 8X8

The output of this contain the amplitude and frequency of each character as 11 bit binary in such a way that the first 6 bits representing the character(amplitude, RUN)and the remaining 5 bits represent number of occurrence(frequency, LENGTH).Since our input string contain 4 characters, our output contains 44 bits(4*11).Thus the input string with 320 bits is compressed to 44 bits string with a compression ratio of ~7:1(bits).compression ratio is calculated as (input bits/output bits):1.

a1	b1	d2	c60

Fig: output matrix

The compression ratio obtained by RLE is:

Compression Ratio = original size/compressed size : 1

Numerical example:

Two examples of compression using RLE are described:

1. Consider the sequence --- *aabbbddddddzzzzcccc*

This string of characters can be compressed to form --- *2a3b7d4z4c*

The 20-byte original string would only require 10 bytes of data to represent the string. In this

case, RLE yields a compression ratio of 2 : 1

2. Consider the string of numbers as follows --- 2, 0, 1, 2, 0, 1, 2, 0, 1

This string can be compressed to form --- 3 (2,0,1). Giving a compression ratio of = 9/4 : 1,

almost 2 : 1.

RLE will not always result in compression. The amount of compression achieved depends on

the data being compressed.

Consider the string --- 1, 2, f, 4, a, a,

After RLE gives --- 1(1),1(2),1(f),1(4),2(a).

To express the original string of 6 bytes, 10 bytes are used. Instead of compression, the original string has expanded.

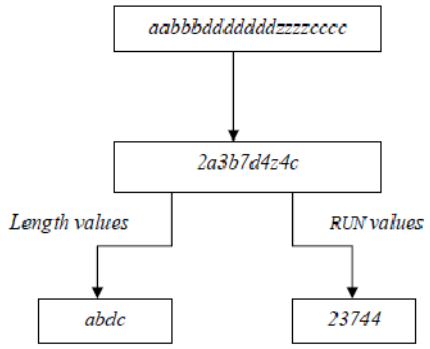


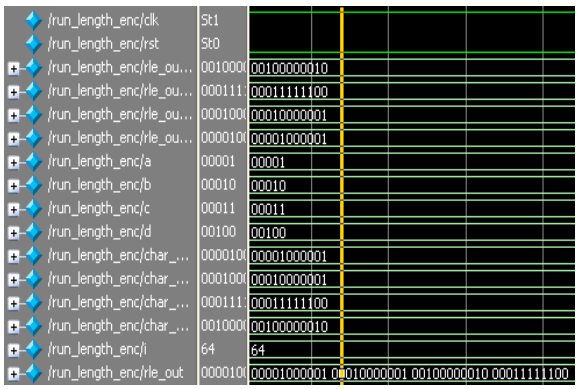
Fig: Flow chart representation

Function Table

Data in	*Clk*	*Rst*	*RLE output*
aaaaab	*1*	*0*	*a3b1*
aaaccbbb	*1*	*0*	*a3c2b3*
sssssshh	*1*	*0*	*s7h2*
haaaaaat	*1*	*0*	*h1a6t1*

Implementation Results:

Simulation Result.

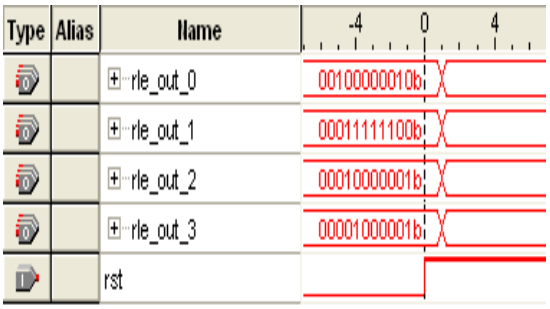


FPGA Prototyping results:

a) Synthesis Result

Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Total logic elements	12 / 33,216 (< 1 %)
Total combinational functions	12 / 33,216 (< 1 %)
Dedicated logic registers	12 / 33,216 (< 1 %)
Total registers	12
Total pins	46 / 475 (10 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

b) Hardware Test Result:



rle_out_0=d2;

rle_out_1=c60;

rle_out_2=b1;

rle_out_3=a1;

c) Power analysis result:

Family	Cyclone II
Device	EP2C35F672C6
Power Models	Final
Total Thermal Power Dissipation	115.23 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	79.94 mW
I/O Thermal Power Dissipation	35.29 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

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SECTION-II

Image Processing and Vision Science

Gray Image Segmentation Based On Fuzzy Theory

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Abstract - Image segmentation, it subdivides an image into its constituent regions or objects. Several algorithms are put forwarded regarding image segmentation, still it remains one of the major difficulties in image processing and analysis. Images or image data more or less have the characteristics of vagueness and ambiguity. It is accepted that fuzzy technique can manage the vagueness and ambiguity efficiently. In this paper an algorithm has been proposed based on fuzzy theory, for segmentation of gray image. The proposed approach firstly maps the image data into fuzzy set which is followed by membership value modification. While through the phases of the proposed approach, the last phase is the defuzzification which is required to bring the fuzzified data into original image data form.

Keywords: *Image segmentation, Fuzzy logic, Fuzzification, Membership function, Defuzzification*

I. INTRODUCTION

Segmentation of an image plays a vital role in computer vision and image processing applications. Over the last few decades the volume of interest, research and development of computer vision and image processing has increased enormously. Since the time of Gestalt [1] movement image segmentation plays a vital role in image processing and computer vision. Images or image data more or less have the characteristics of vagueness and ambiguity which is depends on the devices through which the images are captured and formed. Actually the physical factors of the devices are responsible for the degree of vagueness and ambiguity of data. Because of the presence of characteristics of ambiguity and vagueness in image data, though the degree of presence vary from image to image, it sometimes becomes harder to get the acurate segmentation of an image. These problems can be said as fuzzy in nature. To overcome this problem, the image data can be defined formally in the fuzzy setting in order to take operations that can handle data uncertainty.

The idea of fuzzy set is convenient and natural. Fuzzy technique can manage the vagueness and ambiguity efficiently. [2] States that fuzzy approach for image segmentation can be categorized into four classes: segmentation via threshold, segmentation via cluster, supervised segmentation, and rule based segmentation. Whereas the rule based approaches are applicable for application dependent heuristic knowledge, and able to model them in the form of fuzzy rules.

Set of fuzzy rules are established based on fuzzy variables [3] which are associated with fuzzy c-mean clustering approach (FCM) [4] and the probabilistic c-mean clustering approach (PCM) [5] and construct a correction matrix for modifying the fuzzy partition matrix. In [6], a fuzzy reasoning method in conjunction with a PSO is employed for color image classification through region merging.

Fuzzy logic is a powerful tool to represent and process human knowledge in form of fuzzy if-then rules. The fuzzy theory provides a mechanism for representing linguistic construct such as “many”, “low”, “medium” etc. Consider the meaning of a “dark” for an image whose object X has a gray level value less than 50. For another object Y, which also shares the same image has a gray level value less than 100. This dark is called linguistic descriptor. The term “dark” informs the same meaning to the object X and Y, but it is found that they do not provide a unique definition. The term “dark” would be conveyed effectively, only when a computer compares the given gray level value with the pre-assigned value of the dark. In the proposed approach we have assigned “dark” as a gray value less than or equal to 60, then object having value less than 60 can easily become the member of the set “dark” and value 100 will not be a member of the set “dark”. The membership value is 1 if it belongs to the set or 0 if it is not a member of the set. The above method can be formulated according to [7] as

$$X_A(x) = \begin{cases} 1, x \in A \\ 0, x \notin A \end{cases}$$

Where $X_A(x)$ is the membership of the element x in set A and A is the entire set of the universe. This membership was extended to posses various “degree of membership” on the real continuous interval [0, 1]. Fuzzy sets as the set on the universe X which can accommodate “degree of membership”.

Fuzzy set theory assigns a membership degree to all elements among the universe of discourse according to their potential to fit in some class. The membership degree can be expressed by a mathematical function $\mu_A(x_i)$ that assigns , to each element in the set, a membership degree between 0 and 1. If X is the universe of discourse and x_i an element of X. A fuzzy set A in X is defined as [7]

$$A= \{(x_i, \mu_A(x_i))|x_i \in X\}$$

Where

$$\mu_A : X \rightarrow [0,1]$$

is the membership function of A in X. We say A is non-empty if there exists $x \in X$ such that $\mu_A(x) \neq 0$. Suppose an image whose object X has a gray level value less than 40. For another object Y, which is in the same image has a gray level value less than 70. If to segment a "dark" object from the two objects from an image, it appears to be indurate as both the objects has more or less the properties of being "dark". This can be said as a grayness ambiguity, where as there are too other kinds of imperfection, i.e. geometrical fuzziness, vague knowledge of image feature and many more that exists or came to be as while during the operations of image processing. By considering the above if mapping can be done on the image data into fuzzy set I.e. to fuzzify the pixel values of the original image, the image pixel values can be converted to binary values, between interval [0, 1]. The image pixel values of any size will take the value between [0, 1]. This way the computational can be made easy on binary image. The pre-defined value which in the proposed approach considered as membership value, can be compared with the fuzzified pixel values of being "dark". By considering the pre-defined value, with a membership modification value, can assign a value for each pixel either as "dark" or less "dark". That is if we take the pre-defined value 0.4, then the pixel values in the image those are less than 0.4, can be assigned as "dark, and else less "dark" may be assigned for other pixels where the criteria is wrong . Since fuzzy logic is a powerful tool to represent in form of fuzzy if-then rules, it eases the impediment to recognize of being "dark" and less "dark" between an object. The membership value of being "dark" are represented as in one category of object and the membership value of less "dark" is represented to another category of object. By knowing the "dark" and less "dark" it is easy to segment an image where there are multiple objects present.

II. METHODOLOGY

The methodology adopted as by general implementation of filtering an $M \times N$ image which is resize to $m \times n$ image with a weighted averaging filter given by [8].

$$g(x, y) = \frac{\sum_{s=-a}^{a} \sum_{t=-b}^{b} w(s, t) f(x + s, y + t)}{\sum_{s=-a}^{a} \sum_{t=-b}^{b} w(s, t)}$$

In grayscale image, pixel values are ranges between 0 to 255. The fuzzification technique proposed here is to fuzzify the image pixel values by dividing each pixel value by 255, because 255 is the scale value of gray scale image. After the division, the pixel values are in ranges between 0 and 1. According to fuzzy theory, fuzzy set assigns a membership to all elements among the universe of discourse according to their potential to fit in some class. The membership value here is defined by taking the mean value as the limit of fuzzy set. As all the pixel values is between 0 and 1, the upper limit of the value is taken here as 1 and lower limit as 0, by simple method the value of membership define is evaluated $\mu_m = \frac{P_{UL} - P_{LL}}{2}$, where μ_m is membership define, P_{UL} and P_{LL} is the upper limit and the lower limit of fuzzy pixels value respectively. As in the second step membership define is followed by the membership modification, by considering the value of membership defines (μ_m) as midpoint for membership modification and this is evaluated by the following method:

If $f_z(g(x_i, y_j)) < \mu_m$,

then $f_z(g(x_i, y_j)) \longrightarrow 0$

by the equation;

$$f_z(g(x_i, y_j)) = \mu_m \times \left(f_z(g(x_i, y_j)\right)^2$$

Otherwise if $f_z(g(x_i, y_j)) > \mu_m$

then $f_z(g(x_i, y_j)) \longrightarrow 1$

by the equation

$$f_z(g(x_i, y_j) = 1 - \mu_m \times [1 - \{f_z(g(x_i, y_j)) \}]^2$$

The resultant matrix is the segmented image which is binary.

i.e. $b_z(f(x, y)) = f_z(g(x, y))$

The segmented image contains the object but to get a clear visual description of the segmented object gradient sobel operator has been used to find the edges of the objects. After applying the sobel operator it has been noticed that there are few region belongs to same object which are not connected and to overcome from this

effect another algorithm has been used for finding the connected components of the extracted object. The connected component is found out by the expression given;

$$\bigcup_{i=1}^{n} C_i(e_z(f(x, y)) = C(e_z(f(x, y))) \ldots(1)$$

$$C_i \cap C_j = \Phi \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(2)$$

Equation (1) indicates that the segmentation is complete; when every component is in the region. Where C_i indicates that the component in a region must be connected in some predefined form. And the equation (2) states that two separate region must be disconnected.

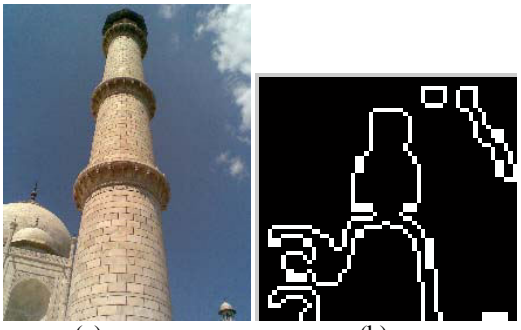
III. RESULTS AND DISCUSSION

On execution of this proposed methodology the results obtained are given as snapshots below. Figure 1(a) shows the original image where the gray level discontinuity between the background and foreground are not very significant and after applying the proposed methodology the segmentation has been done very accurately as every region can be seen

(a) (b)

Figure 1: (a) Original Image. (b) Segmented resized image after using proposed method

Figure 2(a) is the image where intensity between the background and foreground is significant and we can see the segmentation after applying the proposed method.



(a) (b)

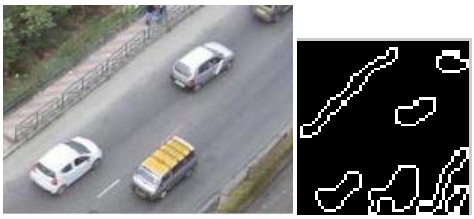
Figure 2: (a) Original image. (b) Segmented image

(a) (b)

Figure 3: (a) original image (b) segmented image

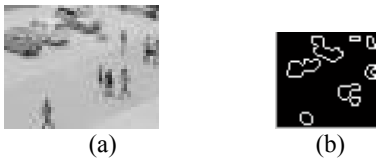
Figure 3 is a image where the intensity discontinuity between background and object is very low as compared with previous images geven here and segmentation has been made by using the above proposed methodology.

Figure 4 and 5 is a image where there are multiple objects were present with objects of variable size and as we can see after applying the proposed fuzzy method segmentation has been made.



(a) (b)

Figure 4: (a) Original image (b) segmented image



(a) (b)

Figure 5: (a) Original image (b) segmented image

IV. CONCLUSION

Because of the uncertainties that exist in many aspects of image processing, fuzzy processing is desirable. While through the study of fuzzy theory and image processing, and how the fuzzy theory can be imposed in image processing especially in the segmentation process, it can be concluded that the applying fuzzy theory in image processing is powerful tool to deals with uncertainty which the previous methods doesn't take into account. In this work an efficient method is provided to find the threshold point by using fuzzy theory. By testing with some of the images the threshold point detected are accurate and by proceeding with the work we get a segmentation of an image which is satisfactory. Thus from the proposed work it can be said the results obtained conclude that the using of fuzzy theory in image processing operation leads to new era and provides a mechanism to deals with problem faced during image segmentation process.

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An Unsupervised Approach to Segment a Color Image through Construction of Multi-Scale Image Towers and using Spatial Constrained K-Means Algorithm

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Abstract **-** Segmentation can be considered as the first step and key issue in object recognition, scene understanding and image understanding. Applications range from industrial quality control to medicine, robot navigation, geophysical exploration, and military applications. In all these areas, the quality of the final result depends largely on the quality of the segmentation. An accurate color image segmentation algorithm can be obtained by considering human being's perception of color. In this paper, we propose an unsupervised approach to segment color image. This approach considers the spatial distribution of colors as perceived by humans and combines the texture and color features to obtain image segmentation that conveys semantic information. This approach produces segmented image which is almost similar to the one produced by human vision system.

Keywords - *Color histogram, CIE-Lab space, Euclidean distance, probabilistic assignment, spatial distribution.CIE - International Commission on Illumination, Lab – color opponent space with dimension L for lightness, a and b for the color-opponent dimensions.*

I. INTRODUCTION

Segmentation of color image is a major field of research in computer vision. Various structural, statistical and spectral approaches have been proposed towards segmenting a color image.

In research paper [1], Mirmehdi & Maria Petrou have described an approach for perceptual segmentation of color image. A multi scale representation of the image, generated by a multi-band smoothing algorithm based on human psychophysical measurements of color appearance is used as an input. Initial segmentation is achieved by applying a conventional k-means clustering algorithm to the image at the coarsest level of smoothing. The segmented clusters are then reconstructed in order to isolate core clusters or patches in which the pixels are definitely associated with the same region. The image pixels representing the core clusters are used to form 3D color histograms which are then used for probabilistic assignments of all other pixels to the core clusters to form large clusters and categorize the rest of the image. The process of setting up color histograms and probabilistic re-assignments of the pixels to the clusters is then propagated through finer levels of smoothing until a full segmentation is achieved at the highest level of resolution.

In research paper [2] a novel K-means based approach is proposed which combines spatial constraints with k-means clustering. K-means based clustering is employed in feature space. In each level of K-means clustering, region growing of the pixels belonging to the same feature cluster is performed to produce a set of labeled image regions. Then, the K-means algorithm on the next level is carried out on these regions separately.

In research paper [3], Chen, Pappas, Mojsilovic and Rogowitz have presented an image segmentation algorithm which is based on spatially adaptive texture features. Two types of features are developed. One describes the local color composition, and the other the spatial characteristics of the grey scale component of the texture. These features are first developed independently, and then combined to obtain an overall segmentation. Adaptive clustering algorithm is used to separate the image into smooth and textured areas and to combine the color composition and spatial texture features to consolidate textured areas into regions.

In research paper [4], Karoui, Fablet, Boucher, Augustin have addressed a multi-class texture segmentation by proposing a novel unsupervised region based criterion. This criterion relies on the maximization of a weighted sum of Kullback-Leibler measure between distributions of local texture features associated to the different image regions. Hence, the segmentation issue is stated as the maximization of the proposed criterion and a regularization term that imposes smoothness and regularity of region boundaries. The proposed approach is based on curve evolution techniques and is implemented using level-set methods.

In research paper [5], a new color image segmentation algorithm by unsupervised classification

of pixels is proposed. This procedure iteratively constructs the classes by multi-thresholding of histogram. For this purpose, the procedure selects different color spaces in which the modes of the histograms are possibly separated so that each mode corresponds effectively to a region in the image.

II. PROPOSED METHOD

In this paper, an unsupervised approach to segment a color image is proposed. The initial motivation for the proposed approach came from the segmentation method proposed by Mirmehdi and Petrou [1] and Spatial Constrained K-means clustering algorithm proposed by Ming Luo, Yu-Fei Ma and Hong-Jiang Zhang [2].

In the method proposed by Mirmehdi and Petrou [1], initial segmentation is obtained by using conventional K-means clustering algorithm. The spatial constrained K-means clustering algorithm proposed by Ming Luo, Yu-Fei Ma and Hong-Jiang Zhang [2] considers the spatial constraints which are essential attributes of images, whereas conventional K-means algorithm considers only cluster observation vectors in feature space. Also spatial constrained K-means clustering algorithm does not lead to over segmentation whereas conventional K-means algorithm leads to over segmentation. Therefore, spatial constrained K-means algorithm is better than the conventional one.

The principle of the approach proposed in this paper is similar to the segmentation method proposed in [1], except that the initial segmentation is achieved by using spatial constrained K-means clustering algorithm [2] instead of conventional one. Thereby the approach proposed in this paper considers the essential attributes of images and avoids over segmentation.

III. DESIGN APPROACH OF PROPOSED METHOD

Initially, a multi-scale representation of input image is generated. Then the initial segmentation of image into clusters is performed at the coarsest level using spatial constrained k-means clustering algorithm. The resulting small clusters are merged based on Euclidean distances of segment boundaries. Then the core clusters are derived from the merged clusters. Then 3D color histograms are constructed from core cluster pixels and are used for probabilistic assignment of all other pixels to core clusters to form larger clusters. This process of setting up histograms and probabilistic reassignment of pixels to clusters is propagated through finer levels of smoothing to obtain full segmentation.

Detailed explanation of segmentation method is as follows.

A. Multi-scale representation of Image

A causal, multi-scale tower of image versions based on perceptual considerations is constructed by using the concept given in [1]. A multi-scale tower of image versions is constructed in order to consider the response characteristics of the human visual mechanism which are functions of not only the spectral properties of the stimuli, but also of the temporal and spatial variations of these stimuli. So when an observer deals with multicolored objects, with fine textures, their color matching behavior is affected by the spatial properties of the observed pattern.

Furthermore, the human visual system will experience loss of detail at increasing distances away from the object. It perceives colored textures at a large distance as areas of fairly uniform color, whereas variations in luminance, e.g., at the borders between two textured areas, are still perceived. Therefore, it is necessary to introduce a multi-scale smoothing algorithm that smoothen an image according to human perception

So an algorithm is constructed which smoothens the image in luminance and chrominance color planes separately with different filter matrices for the planes. In this algorithm, the opponent color space is used which consists of three different color planes, O1, O2, O3, representing the luminance, the red-green, and the blue yellow planes, respectively. In the O1, O2, O3 color space, each of the planes is smoothed separately with two-dimensional spatial kernels, defined as sums of Gaussian functions with different values of standard deviation σ. The result of this operation is that the luminance plane is blurred lightly, whereas the red-green and the blue-yellow planes are blurred more strongly. This spatial processing technique is pattern-color separable.

In order to apply this algorithm on the input image, the input RGB (red, blue, green) image is transformed into the O1, O2, and O3 opponent color space. Then the image is smoothened. After this the image data is transformed from the O1, O2, O3 to the CIE-Lab space, which is a perceptually uniform space and, therefore, more suitable for carrying out color measurements.

B. Initial Segmentation of Image using Spatial constrained K-means clustering algorithm

A spatial constrained k-means algorithm proposed in [2] is used to initialize the segmentation at the coarsest level of image. The goal of k-means algorithm is to partition the observations (X_i; i=1…L) into k-groups with means $\overline{X}_1, \overline{X}_2 \ldots \overline{X}_k$ such that

$$D(K) = \sum_{i=1}^{L} \min_{1 \le j \le K} (X_i - \overline{X}_j)^2 \qquad (1)$$

is minimized. The observation vector X_i used in the proposed method is the vector containing the x, y co-ordinates of the pixels and Lab color space values of the pixels. In spatial constrained K-means algorithm, on each level of K-means clustering, a region growing of those pixels belonging to the same feature cluster is performed through a connected-components algorithm to produce a set of labeled image regions. Then, the K-means algorithm on the next level is carried out on these regions separately.

The initial set of means which is chosen are simply a randomly distributed set of points in the (x, y, L, a, b) space. During each iteration, the Euclidean distance between each of the pixels and centroid of clusters are calculated. Then the pixels are assigned to the cluster whose centroid is at minimum distance from the pixel. Then, region growing is performed only in clusters to which the pixels are assigned. Then the centroids are determined for these clusters based on XY coordinates and Lab color space values of the pixels which give its spatial characteristics. This process continues until the centroids are stabilized.

C. Merging of Clusters

After the initial segmentation, the small clusters are merged based on concept given in [1]. Each pair of regions with a common border is tested for merging. The average Lab color of the border pixels for each of the two regions is computed. If this Euclidean distance of these two Lab colors is less than a certain threshold, the two regions are merged. The merging process stops when no pair of regions that can satisfy the merging criterion can be found. Then the area occupied by each of the merged clusters in the total image is determined. If this is less than the pre-defined threshold, the corresponding clusters are removed.

D. Core Clusters

The core clusters describe groups of pixels which can be confidently associated with the same region of texture in the image. The core clusters are derived from initial clusters, based on the concept given in [1]. The standard deviation σc is calculated for each cluster c; c =1,…C, where C is the total number of clusters. Then, every pixel is associated with a confidence p_c^i which is calculated as follows

$$p_c^i \equiv \frac{\dfrac{\sigma_c^2}{d_c^{i^2}+\sigma_c^2}}{\dfrac{\sigma_1^2}{d_1^{i^2}+\sigma_1^2}+\dfrac{\sigma_2^2}{d_2^{i^2}+\sigma_2^2}+\cdots\cdots+\dfrac{\sigma_c^2}{d_c^{i^2}+\sigma_c^2}} \forall i, \forall c \qquad (2)$$

where $d_1^{i^2}$ is the squared distance of pixel i from the mean of cluster c in Lab color space. Each core cluster is formed from the pixels that can be associated with it with a confidence of at least 80 percent.

E. 3D Color Histograms and update of Probabilistic assignments

The core clusters formed at resolution level l+1 are mapped back into the image at resolution l and, using the color pixel values in those regions, a three-dimensional color histogram is set up (dynamically) for each region by using the concept given in [1]. This provides a statistical characterization for each different texture at each resolution. From these color histograms, the likelihood of a pixel i at smoothing stage l to have label ω_k can be calculated using the color of that pixel. This likelihood is represented by $P(x_i^l \mid \theta_i = \omega_k)$ …(3). In this manner, the distribution of the features that characterize a texture at each resolution level can be derived.

At all other levels l < L (where L is the total number of levels), the probability label assignments for each pixel at level l+1 is computed using the below mentioned formula.

$$P(\theta_i = \omega_c \mid x_i^L) = p_c^i \forall i, \forall c \qquad (4)$$

IV. RESULTS

The segmentation result of the images shown in Figure 1a, 2a &3a using the method given in [1] is shown in the figure 1b, 2b & 3b and using the proposed method is shown in Figure 1c, 2c & 3c.

It can be seen from the figures 1c, 2c & 3c that segmentation results obtained from the proposed method is not over segmented, it is almost similar to the image segmentation performed by human vision system and it is better than the segmentation results obtained by using the method given in [1].

V. CONCLUSION

In this paper, an unsupervised approach to segment color image that considers the spatial distribution of colors as perceived by humans is proposed. This is performed by constructing a causal, multi-scale tower of image versions based on perceptual considerations. The initial segmentation on coarsest level of image is achieved by using spatial constrained k-means algorithm which considers the essential attributes of images, avoids over segmentation and better than the conventional one. The resulting clusters are merged if the merging criterion is satisfied. Core clusters are

derived from these merged clusters. The core clusters formed at resolution level l+1 is mapped back into the image at resolution l and, the color pixel values in those regions are used to set up a three-dimensional color histogram for each region. This provides a statistical characterization for each different texture at each resolution which refines the segmented clusters to provide better results. The resulting segmented image closely matches with the one which is obtained as a result of segmentation performed by human vision system.

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Fig. 1 (a)

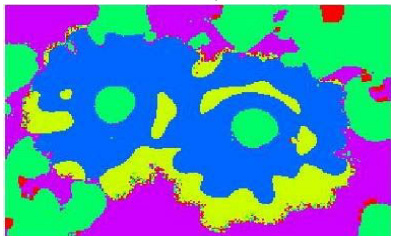

Fig. 1 (b)

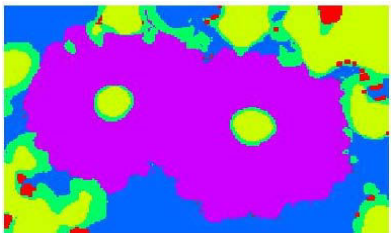

Fig. 1 (c)

Fig. 2 (a)

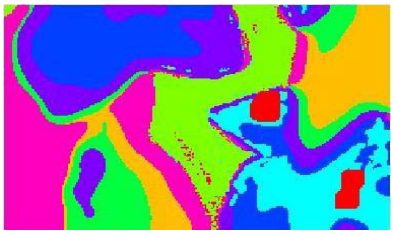

Fig. 2 (b)

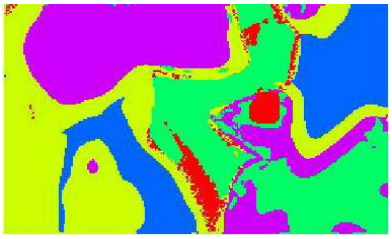

Fig. 2 (c)

Fig. 3 (a)

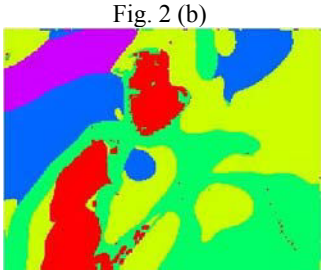

Fig. 3 (b)

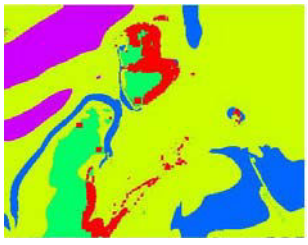

Fig. 3 (c)

Fig. 1a, 2a & 3a are all original color images, Fig. 1b, 2b & 3b are all the segmentation results obtained by using the method proposed in [1], Fig. 1c, 2c & 3c are all the segmentation results obtained by using the proposed method.

Real-Time Visual Odometry Using Monocular Camera

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Abstract - Various methods of estimating the motion of a monocular camera have been studied in literature and proposed as candidate solutions for vision based navigation. Of these, Visual Odometry that estimates incremental motion from matched features in every pair of successive images is attractive for its simplicity. This paper presents a real time implementation of monocular visual odometry on a laptop with a graphics processor. The algorithm based on Ransac and Nister's 5 point algorithm is discussed. The performance of the implementation is tested using static and dynamic tests.

Keywords - *Vision based navigation, GPU SURF, 5 point algorithm, Ransac.*

I. INTRODUCTION

Visual odometry is the process of estimating the position and orientation of a vehicle or sensor platform using image data from an on-board camera. The position and orientation measurements or estimates can be used for guiding and controlling the vehicle to carry out required tasks.

In odometry, the vehicle position and orientation at each instant in time are calculated using a dead reckoning procedure – i.e. by starting with known values and integrating incremental translation and rotation computed from every pair of successive frames. The translation and rotation between two frames is computed using algorithms based on multi-view geometry.

In this paper, we present one method for visual odometry based on Ransac and the 5 point algorithm, focusing on real-time implementation of the method on a laptop. A graphics processor available on the laptop is used to execute the image processing computations enabling the algorithm to be executed in real-time. An experimental method of characterizing the performance of the system is also discussed.

Sections II and III describe the details of the odometry algorithm and the real -time implementation respectively. Section IV presents experimental results of camera orientation determined using the method and discusses the method of characterizing the angular accuracy of this scheme.

II. THE ODOMETRY ALGORITHM

A visual odometry algorithm takes as input the list of feature matches corresponding to a pair of images and computes the relative orientation and position between the two cameras. The relative orientation is expressed as a 3x3 rotation matrix R and is uniquely computed. The rotation that describes the relative orientation can also be expressed in terms of the 3 Euler angles that can be computed from the rotation matrix R. The relative position is expressed as a translation vector T measured with respect to the reference frame of the first camera and can be computed only upto a scale factor. In a sequence of images acquired from a monocular camera, the incremental rotation and translation corresponding to each pair of frames is integrated to compute the absolute orientation and position of the camera. Several methods of computing R and T given a pair of images have been suggested in literature [1]. The work presented here uses Nister's 5 point algorithm [2] to find Euler angles and a translation vector by using a minimum of five matched points between two views of a calibrated camera. The 5 point algorithm can also be used with more than 5 matched features to give a least squares estimate of the relative position and orientation.

Since the set of feature matches is likely to include a small percentage of bad matches or outliers, some form of search or optimization procedure is required to estimate the best R and T that fits the given set of matches. The most popular method for such scenarios is the random sample consensus algorithm (Ransac). This procedure consists of repeatedly picking random subsets of the data and evaluating a chosen cost function with the subset to evaluate its score. After several such iterations, the random subset with the highest score is assumed to be the best fit and the data points that agree with the best fit are picked as the inliers.

In case of visual odometry, Ransac is used in conjunction with the 5 point algorithm and a distance error that is computed for each trial solution and compared to a threshold to decide the score of the trial.

A fixed number of random trials (in our case about 500) are performed and the best sample from the random trials is used to compute an estimate of rotation and translation R and T. This is followed by a refinement procedure wherein a further fit is performed with all the inliers of the best random sample. The corresponding R, T are again evaluated using a threshold on the distance error to compute the number of inliers. If no improvement in the number of inliers is seen as compared to the best fit from the basic Ransac procedure the refined values of R, T are discarded. Thus, the refinement stage tries to widen the consensus to achieve better results. Multiple stages of refinement can be used.

The Euler angles can be extracted from the 3x3 rotation matrix R as follows:-

$$\varphi = \tan^{-1}(R(2,3)/R(3,3)) \quad (1)$$

$$\theta = \sin^{-1}(-R(1,3)) \quad (2)$$

$$\psi = \tan^{-1}(R(1,2)/R(1,1)) \quad (3)$$

where $R(i,j)$ refers to the i,j^{th} entry of the rotation matrix R and φ, θ, ψ represent the roll, pitch and heading angles of the camera respectively respectively. The experimental results for computation of these Euler angles are presented in section IV.

III. REAL-TIME IMPLEMENTATION

The scheme used for real-time implementation of the odometry algorithm in this work is described in this section. It is illustrated in Figure 1. The shaded block in figure 1 indicates the part of the algorithm executed on the graphics processor, in this case GPU SURF.

The various steps of the complete algorithm are described below.

A. Image Acquisition and SURF Feature Extraction

Images were acquired from the calibrated camera. Point features are extracted out of these images using the Speeded-Up Robust Features (SURF) algorithm.

The odometry algorithm is executed at 8 frames per second. As SURF is a very computationally intensive algorithm, running it on standard laptop at 8 Hz is difficult. A Graphical Processing Unit (GPU) available on the graphics card on a PC/laptop can be used to accelerate the feature extraction process by using the parallel architecture of a GPU. In this work, a GPU implementation of SURF was used from the work presented in [4] which primarily focuses on methods of using the parallelism afforded by a GPU to optimize the SURF algorithm. This implementation exploits parallelism in image space as well as scale space to minimize the run time of SURF on the GPU.

The use of GPU SURF enables the feature extraction computations to be performed on the graphics processor while the rest of the odometry algorithm is executed on the main processor of a laptop. This sharing of load enables execution of the complete algorithm at 8Hz.

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Fig. 1 : Block diagram of the odometry computations

The SURF algorithm computes features along with descriptor vectors for the features which are essential for matching features between frames.

B. Feature Matching

After the SURF features have been extracted, feature matching is performed by trying to get descriptors which are as similar as possible between consecutive images.

The matching process uses the Euclidean distance between the descriptor vectors of two candidate features. Each feature from the first frame is compared against every feature from the second frame using this distance. The feature from the second frame that gives the minimum distance is chosen as the matching feature. In case this minimum distance is above a pre-determined threshold the feature from the first frame is discarded.

C. Normalization & Distortion Correction

The camera used for the purpose of the work presented here has to be calibrated in advance. This was done by using the calibration toolbox for MATLAB [3]. This process estimates the intrinsic calibration parameters of the camera and the coefficients of the distortion model that are used to correct the feature

coordinates as described below. This is an off-line process that generates values of the calibration parameters used in the odometry algorithm.

The 5 point algorithm normalized image co-ordinates of the matched features. This is achieved by multiplying the image pixel co-ordinates with the inverse of the camera calibration matrix obtained from the off-line camera calibration before they are fed into the model.

The presence of distortion in the camera can result in large errors or poor performance of the algorithm. The off-line calibration procedure provides an estimate of the polynomial coefficients of the distortion model. Elimination of the distortion can be performed either by rectification of the image before feature extraction or by applying a distortion compensation to the feature coordinates after feature extraction. In our case we follow the latter method. The distortion model used is a sixth order distortion polynomial.

D. Ransac and Refinement

The odometry algorithm was implemented in a Simulink model. Matlab Real Time Workshop was used to generate C code from the Simulink model. The generated code provides a function containing a single time step of the entire algorithm modeled in Simulink and shown in figure 1. A simple code wrapper developed in C is used to call GPU SURF and the step function. The features obtained from GPU SURF are processed using the matching algorithm described in sub-section B. The set of feature matches are then provided as an input to the step function. The function provides the rotation matrix between the current and previous frames. This rotation matrix is the integrated and converted into the Euler angles using equations (1)-(3).

E. Integration

The incremental rotation and translation obtained from the Ransac algorithm are transformed to the reference frame. In our case the initial camera frames is used as the reference frame for the entire trajectory. A local level or NED frame can also be used if the initial orientation of the camera is known. The incremental rotation is then transformed into incremental Euler angles using equations (1) – (3) and then integrated to obtain the absolute orientation of the camera.

IV. EXPERIMENTAL RESULTS

In this section we analyze the errors in the absolute orientation of the camera computed by the odometry algorithm. The position computed is only unique upto a scale factor, it was not attempted to check the position accuracy.

The video odometry depends on the integration of incremental rotation between each pair of camera frames, and each incremental rotation has a random error. Hence a slow drift is seen over time in the values of the absolute orientation reported by the algorithm.

As explained in the previous section, each absolute angle is obtained by summing the incremental angles at each time step. Further, since each incremental angle measurement is likely to have a small error, the error in the absolute angle keeps increasing with time which can be described as a random walk. If the error in incremental angle at each frame ε is assumed to be a zero mean Gaussian random variable with standard deviation σ_ε the standard deviation of the error in heading angle ψ after n frames is given by $\sqrt{n}\ \sigma_\varepsilon$.

The drift in the angles computed by the odometry algorithm can be characterized experimentally under static and dynamic conditions. The same process can be used to check the accuracy for all the 3 Euler angles.

A. Characterization of error under static conditions

It was first attempted to measure the drift in the angles reported by odometry under static conditions. This was done by taking 20 one minute runs while the camera was kept absolutely stationary. The odometry algorithm was run at 2Hz. The results were over-plotted to represent them concisely. Since the actual change in angles is zero, the plot also represents the errors in the corresponding angles. Figures 2, 3 and 4 depict the errors in roll, pitch and heading angles over the 20 runs.

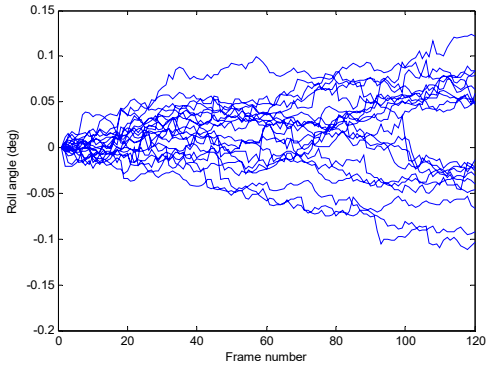

Fig. 2 : Roll angle from odometry in static conditions

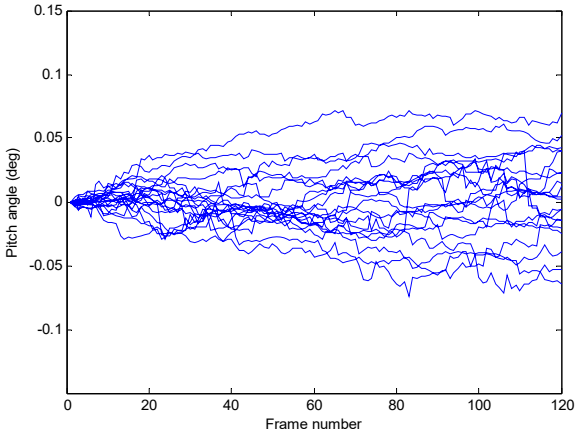

Fig. 3 : Pitch angle from odometry in static conditions

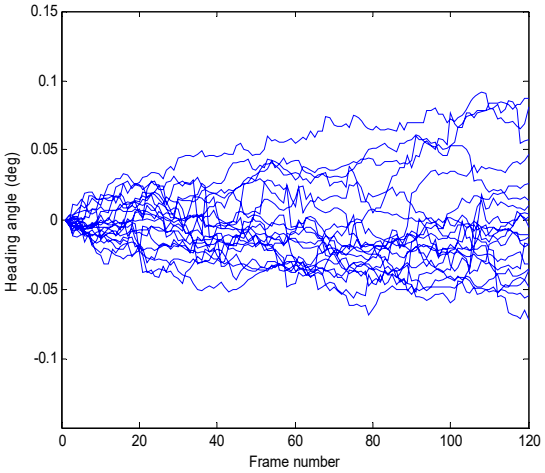

Fig. 4. : Heading angle from odometry in static conditions

Table 1. Standard Deviation of error in Euler Angles at the end of 1 minute under static conditions.

Angle	Standard Deviation after 1 minute in degrees
Roll (φ)	0.0649
Pitch (θ)	0.0354
Heading (ψ)	0.0434

For a static run, the true angles are known at all points in time. Hence we can also calculate the statistics of the error in each frame ε. The mean value of ε indicates whether the errors are unbiased. For the above static runs, the mean value was seen to be under 1.3e-4 for all the three angles which indicates negligible bias. The standard deviation of ε, σ_ε , can be used to calculate the standard deviation of error in absolute angle after n frames as $\sqrt{n}\ \sigma_\varepsilon$.

Table 2. Standard Deviation per frame for errors in Euler Angles

Incremental Angle	Standard Deviation (degrees)
Roll (φ)	0.0048
Pitch (θ)	0.0036
Heading (ψ)	0.0045

B. Slow dynamic test with ground truth

The next test was carried out to measure the accuracy of the computed Euler angles with a known amount of angular motion of the camera. To test this, the camera was mounted on a positioning table that can be manually rotated through a known angle in each axis. The camera was rotated in steps at 15° intervals through +/- 60 degrees for roll and pitch angles and through +/- 90 degrees for the heading. The Ransac method is used to compute the absolute orientation of the camera and compared to the ground truth read out from the positioning table. The errors were seen to lie within +/- 2 degrees over the entire range of variation in the 3 angles. However, since the temporal aspect was not considered the results are of limited use in analysis. Figure 5 shows the result of the heading angle test. As seen, the computed heading angle follows the true value closely with an error of < 2 degrees for the entire range of heading variation.

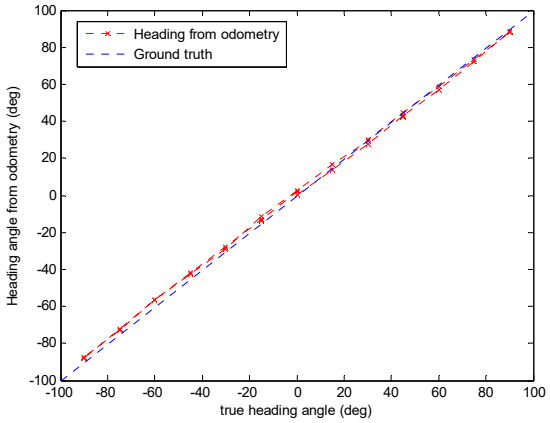

Fig. 5. Heading angle from odometry and ground truth

C. Dynamic Tests

This test is intended to characterize the error build-up while the camera is in motion. 20 dynamic tests were conducted, each of 1 minute duration with the odometry algorithm running at 8Hz. The camera was brought back to its initial position at the end of each run. This enables the error in the final angles to be computed. Ideally, the values of the angles should also return to zero. However

this does not happen because of integration of incremental errors as described above. The error at the end of the 1 minute runs indicates the drift error of the odometry scheme under dynamic conditions. Figures 6, 7 and 8 show the three Euler angles for the 20 runs. As seen the angles do not return to zero at the end of the 1 minute trajectory. This difference from zero is the drift in estimated angles over the 1 minute run.

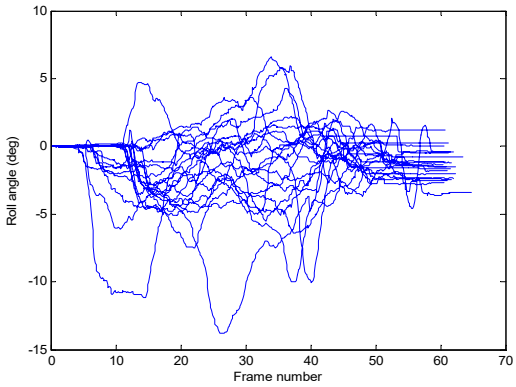

Fig. 6 : Roll angle during dynamic runs

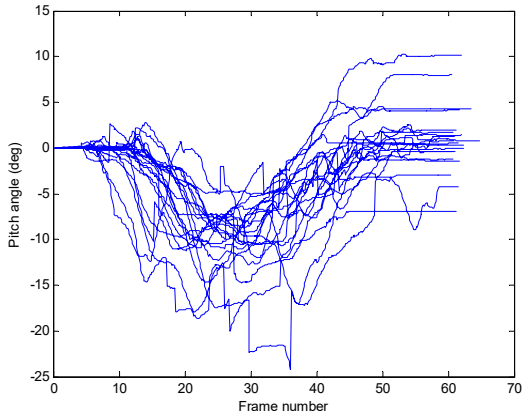

Fig. 7 : Pitch angle during dynamic runs

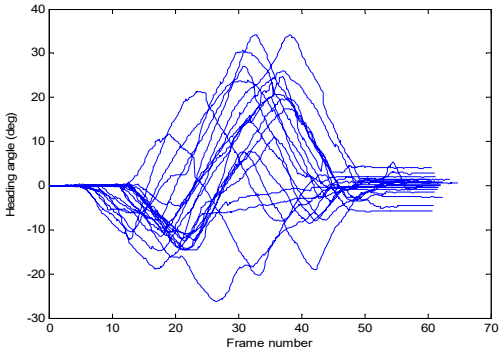

Fig. 8 : Heading angle during dynamic runs

Table 3 shows the standard deviations in the three Euler angles at the end of one minute runs composed of 480 frames.

Table 3. Standard Deviation of error in Euler Angles at the end of 1 minute under dynamic conditions.

Angle	Standard Deviation of the angle error at the end of 1 minute (degrees)
Roll (φ)	1.1353
Pitch (θ)	2.3123
Yaw (ψ)	2.2623

The error per frame (σ_ε) can be calculated for the heading angle as $\sigma_\varepsilon = 2.2623 / \sqrt{480} = 0.103$ deg.

Similarly, the standard deviations for the incremental errors in roll and pitch axes are obtained as 0.051deg and 0.105 deg respectively.

These values can be used to calculate the expected performance of the odometry algorithm.

D. Odometry Performance

The performance metrics in the previous sub-sections show that the angle errors per frame have a standard deviation of 0.005 deg in static conditions and 0.1 deg in dynamic conditions. These numbers can be used to predict the performance of the system for longer runs using equation (5).

For example for a vehicle trajectory of 5 minutes (300 seconds) duration, with the odometry running at 8fps, wherein the vehicle is stationary for 100 seconds and moving for 200 seconds the standard deviation of total error in angles at the end of the trajectory is expected be

$$\sqrt{100*8}*(0.005)+\sqrt{200*8}*(0.1)=4.14\text{deg}$$

V. CONCLUSION

In this paper, we have presented an implementation and testing of real-time visual odometry. The odometry algorithm is implemented on a laptop with the computationally intensive feature extraction step hosted on a graphics processor using GPU SURF thereby enabling real-time execution at fast frame rates. Methods of characterizing the performance of the overall system in terms of angular errors have also been discussed along with sample experimental results. The results show angular accuracies of 0.05 degrees per minute in static conditions and 2 degrees per minute in dynamic conditions. The error per frame σ_ε calculated from the experimental data can be used in estimating the performance of the system for longer trajectories.

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An Optical Approach to Sketched Circuit Simulation

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***Abstract* -** This paper describes the implementation of a setup which can analyze and simulate hand drawn electrical circuits. The setup takes the image of the circuit as the input, recognizes the symbols of the different components, identifies the nodes and then simulates the circuit by automatically creating a simulation netlist in SPICE and executing it. Support Vector Machines(SVM) and Multilayer Perceptrons(MLP) were used as training algorithms to learn the various symbols of circuit components and Histogram of Oriented Gradients was used to extract image features. An algorithm was developed which could identify the circuit nodes and connections based upon the relative positions and orientations of the components in the circuit.

***Keywords* -** *SVM; HOG; Symbol Recognition; Circuit Simulation.*

I. INTRODUCTION

A. Motivation

Over the years different schemes have been devised and implemented to analyze and simulate a given electrical circuit. These include circuit simulating programs such as SPICE and softwares such as MULTISIM. While these schemes prove efficient for large scale complex circuits, they are rather time consuming, hardware dependent when it comes to analyzing small and medium scale circuits. Moreover using these programs require special skills on the part of the user. The method described in the paper would help in bridging the gap between the user and the simulation software and will eliminate the need of learning the specifics of the software.

B. Circuit Symbols

A generic electrical circuit consists of a variety of symbols which are used to denote electrical components. We have focused our work on indentifying the most common of those like resistors, capacitor, inductor and battery. The resemblance between symbols of capacitor and battery as well as those of resistor and inductor make the problem of extracting relevant features rather complex. Moreover, detecting the same symbol in different orientations posed another challenge.

C. Dataset Generation

Though data repositories of electrical symbols can be found, we have generated our own dataset customized to the needs of our application. Samples for different symbols were collected form 20 people to maintain diversity and robustness of the learning algorithm.

D. Approach

The approach followed was to extract relevant features from the standardized dataset. The subsequent step was to build a robust classifier from these features which could achieve a high detection rate followed by devising an algorithm which could build up a virtual picture of the circuit by analyzing the symbol positions and orientations. The final step was to generate a simulation netlist and execute it thereby simulating the circuit.

II. METHODOLOGY

The whole process can be divided into the following components.

a. Training Set Generation

b. Image Preprocessing

c. Feature Extraction

d. Classifier

e. Circuit Analysis and Simulation

A detailed description of these steps is as follows.

A. Training Set Generation

A handwritten dataset was generated for each of the symbols. For standardizing, a template was created on a typical A4 size sheet (size) which consisted of 54 contiguous squares of 200 by 200 pixels each. The symbol was enclosed in the boxes to ensure certain uniformity in size and also to aid in extracting individual samples from a sheet. Samples from 10 different volunteers were obtained to ensure diversity due to varying drawing styles and sizes. The sheets were scanned to extract individual samples. A complete dataset of varying from 250 to 500 was obtained for

each symbol. Also 500 more samples which were random patterns were also obtained as common negatives to all the symbols classes. A dataset containing ~5000 samples was acquired.

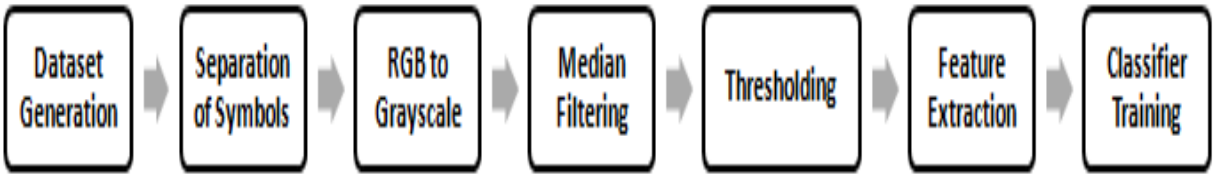

Fig. 1 : Series of steps employed in the training process

B. Image Pre-processing

The scanned images were first converted to grayscale and the individual symbols were extracted. The following noise removal techniques were applied.

(a) Image Resizing

A large part of the image sample remained empty because the written symbols were very small compared to the sample size hence the size was reduced to 150X150 pixels to make the image matrix denser.

(b) Median Filtering

It was used to remove the salt and pepper and speckle noise which result due to the image acquisition process.

(c) Thresholding

To remove any residual irregularities and to increase image contrast, all the image samples were thresholded and this also ensured sharper boundaries.

Following the above steps ensured a clean distinct image with minimal residual noise and sharper contrast.

C. Feature Extraction

A classifier trained on raw pixel data would result in a very huge feature vector. This makes the computation and learning very slow and also yields a high error rate. To overcome the difficulties associated with learning raw pixel data, Histogram of Oriented Gradients (HoG) features were used. This feature set is independent of the image size and captures localized information about intensity gradients.

A MATLAB script computes the HoG of the samples and returns an 81 feature vector. The feature values are scaled to the range of [0, 1].

HoG Parameters

Number of HOG windows per bound box:
Horizontal - 3
Vertical - 3

Number of Bins in Histogram - 9

Filter Kernel:
Along Horizontal - [-1 0 1]
Along Vertical - [1 0 -1]'

Feature Vector Dimension - 81

Fig. 2 : HoG Parameters

*D. **Learning***

(a) Support Vector Machines

SVM's have found widespread acceptance as being one of the best classification algorithm and has been used for numerous object recognition applications. The potential implementations range from face detection to finance. To implement the SVM classifier, LibSVM library interfaced with MATLAB was used and "one against all approach" was followed.

The classifiers were trained using the radial basis function (RBF) kernel. The gamma value ranging from 0.03 to 0.7 was used depending on the type and orientation of the sketched symbol. The values were found using a heuristic approach.

The performance of the classifiers was evaluated using a test set consisting of 200 symbols of each component in the two configurations.

The following table shows the accuracy and other parameters of the SVM classifiers.

TABLE I. Results for the trained SVM classifier

Component	Configuration	No of Iterations	No of Support Vectors	Accuracy (%)
Resistor	Horizontal	314	230	98.2321
Resistor	Vertical	713	450	97.1131
Inductor	Horizontal	383	281	97.6137
Inductor	Vertical	435	286	97.6492
Capacitor	Horizontal	319	219	98.3026
Capacitor	Vertical	366	260	98.1646
Battery	Vertical	190	136	97.8798

(b) Multi Layer Perceptron

Multilayer perceptrons using a back-propagation algorithm are the standard algorithm for any supervised-learning pattern recognition process and the subject of ongoing research in computational neuroscience and parallel distributed process. To implement the MLP neural network, Neuroph 2.5.1 library in Java2 SE was used and the corresponding training set was provided by Matlab which was interfaced to the Java environment using the JMatIo library.

A network consisting of two layers with 81 units in the hidden layer and 1 unit in the output layer was used for this purpose. As per the convention, a sigmoid activation function was used in each neuronal unit to compute the output. A learning rate of 0.7 was used heuristically. Like in the case of SVM, the performance of the networks was analyzed using a test consisting of 200 symbols of each component in the two configurations.

For comparison purposes the number of iterations was kept similar to those of SVM.

The following table shows the test set accuracy of the networks trained for the symbols.

TABLE II. Results for the trained MLP classifier

Component	Configuration	No of Iterations	Accuracy (%)
Resistor	Horizontal	314	97.8420
Resistor	Vertical	713	96.4289
Inductor	Horizontal	383	96.1137
Inductor	Vertical	435	95.8462
Capacitor	Horizontal	319	96.0053
Capacitor	Vertical	366	96.5109
Battery	Vertical	190	94.6221

E. Circuit Analysis and Simulation

A sliding window detector for identifying and localizing circuit components is used initially. The circuit elements which are detected from the previous stage are stored in a Matlab file sorted by their x co-ordinate. The file contains each detected component's x and y co-ordinates as well as the component type and orientation. All the components which have a difference of less than sliding window size in their x or y co-ordinate from the previous component in the list get removed to avoid repeated detection. Then, a heuristic estimate of a y co-ordinate separating the circuit in two vertical halves is calculated and this measure along with the component type, their orientation and their co-ordinates are used to assign nodes to the components. It is ensured that all connections are made exactly as in the original circuit diagram. Finally, a file is created to store the simulation netlist created for WinSpice using the component list and their assigned node values.

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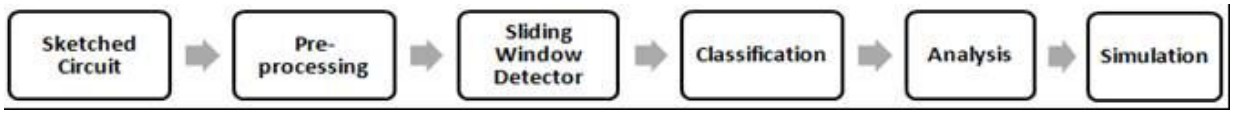

Fig. 3 : Series of steps employed in the proposed method for circuit detection and simulation

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III. RESULTS

A. SVM vs. MLP

The following figures compare the accuracies of the two algorithms. It was observed that SVM classifiers performed better than MLP. This was expected as the SVM algorithm finds the optimum separating hyperplane.

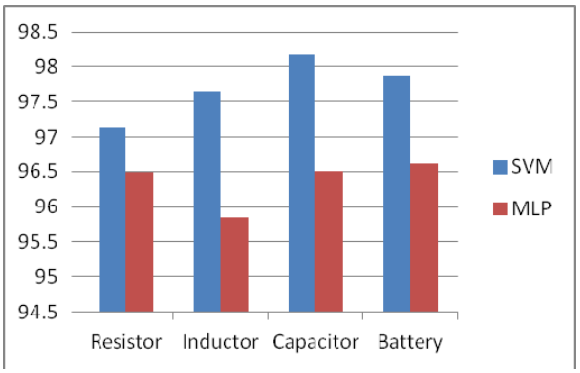

Fig. 4 : Comparision of detection accuracies of both methods for components in vertical orientation

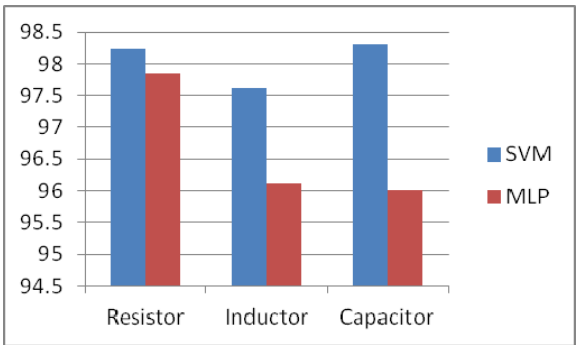

Fig. 5 : Comparision of detection accuracies of both methods for components in horizontal orientation

B. Sketched Circuits

Till now, the classifiers were tested on individual symbols. To analyze the performance on hand drawn circuits, samples were obtained from volunteers which consisted of circuits having different combinations of elements. The number of elements in the circuit varied from 1 to 6. A set of 20 sample circuits were obtained for each number from 1 to 6 making the total dataset of 120 circuits. The standard preprocessing steps similar to the ones used in case individual symbol samples were applied.

Using the sliding window detector described in the previous section, the circuit samples were analyzed. The values of the symbols such as resistance(ohms), capacitance(farad), inductance(henry) and voltage(Volts) were obtained from the user using a Java based GUI.

The following graph illustrates the number of circuits simulated correctly. X – axis represents the number of circuits and Y-axis represents the number of elements.

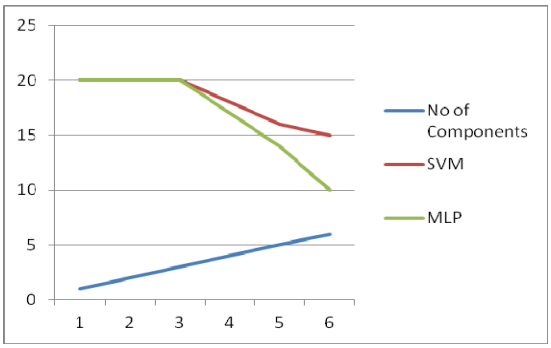

Fig. 6 : Comparision of detection accuracies in sketched circuits

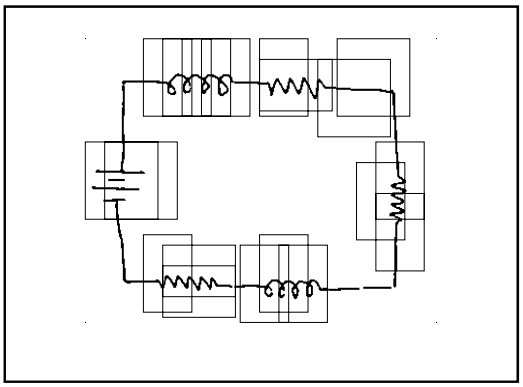

Fig. 7 : Result of analysis on a sketched circuit

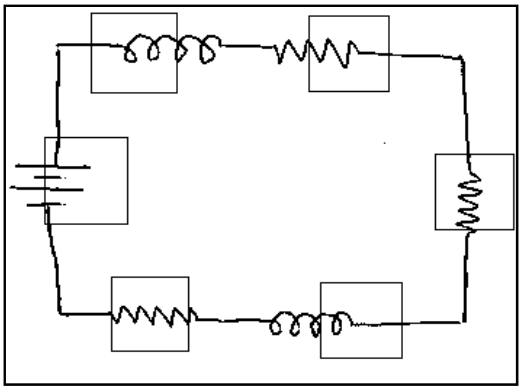

Fig. 8. Result after removing redundant detections

IV. CONCLUSIONS and FUTURE DEVELOPMENTS

The paper has described an innovative method for analyzing hand drawn circuit and brings out a unique application of image processing and machine learning algorithms. HoG has proven to be an efficient way of representing features in the image. SVM is indeed one of the most effcient learning algorithms.

We plan to improve this setup in terms of the acuracy and increasing the number of elements which it could detect. Also we plan to make the setup on line in which live images captured by a camera are analyzed and simuated.

The effciency of the classifier and improvements in the sliding window detector are the primary challenges.

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Estimation of Fractal Dimension by Image Processing Techniques

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Abstract **-** Image processing techniques such as Autosignal and Fractalyse to calculate fractal dimension of fracture surface using ductile and brittle modes of fracture of SS304. Range of fractal dimension is found over these modes. The change in fractal dimension for the variation of pixel count is found in perpendicular directions.

Keywords **-** *image processing; fractal dimension; ductile and brittle fracture.*

I. INTRODUCTION

In the recent times, fractals have been used to describe irregular phenomena in many scientific areas. This includes measuring the length of irregular coastlines. The concept of fractals can be used to study complex shapes of fracture surfaces of materials. In general, fractures, which originate and grow in rocks, metals and concrete, present a ramified and self-similar structure. This means that certain geometrical properties appear at any scale. Reference [1] was the first to introduce fractal character of fracture surfaces of solid materials. In almost all aspects of fracture mechanics of disordered materials, fractal dimensions of fracture surfaces play an important role. So, the fractal geometry is found to be an effective tool in solid mechanics to describe mechanical damage with statistical characteristics.

From a mathematical point of view, self-similar scaling implies a power law satisfied by independent variables. The generic form of many power laws has the form $y=ax^{\alpha}$ which is characterized by two parameters a (the amplitude) and α (the exponent) where the former depends on the choice of the physical quantities involved, and the latter is characterized by the physical process itself, that is, the self-similar property which governs the scaling. When we consider any power-law distribution, it is a mathematically equivalent to a fractal distribution, where the exponent involved has non-integer values. The upshot of this discussion is to determine the fractal dimension of the fracture surfaces. Figure.1 represents the Koch flake with different iterations of self-similarity. Fractal dimension is represented as D which is determined by

$$D=\left|\frac{\log (N)}{\log (k)}\right| \qquad (1)$$

where "N" is the number of self-similar structures of linear size "k" needed to cover the whole structure. Figure. 1 represents Koch flake with different iterations of self similarity. Table I represents parameters to determine fractal dimension of Koch flake.

TABLE I : Parameters to determine fractal dimension

k	N	log(k)	log(N)
1	3	0	0.477121
0.333333	12	-0.47712	1.079181
0.111111	48	-0.95424	1.681241
0.037037	192	1.43136	2.283301

Figure. 2 shows the log-log plot between self similar structures and linear size; based on this data the linear equation of Koch flake is found. It is of form y = mx +c where m is slope which represents fractal dimension.

$$y=-1.261x+0.477 \qquad (2)$$

Hence the fractal dimension of snow flake is 1.261. Figure. 3 shows the macroscopic surface features seen on almost every fatigue surface. The origin is where the crack actually initiated. The crack then grew slowly across the fatigue zone. During this slow crack growth, there are variations in the load that resulted in corresponding variations in the crack growth rate that appear as progression marks. Eventually, the crack reached the point where the material was overstressed, and resulting in overload zone. In the overload zone, most cracks grow as brittle fracture. In ductile and brittle fracture mode, material failure leads to patterns

that depend on the parameters, such as the fractal dimension [2].

The vertical section method is used to calculate fractal dimension for steel failed by impact [3]. Profilometric analysis is introduced to determine fractal dimension on metals [4]. Projective covering method is utilized to determine fractal dimension of ductile and brittle materials [5]. Reference [6] indicated that fractality can be a parameter to judge fracture mode and used laser displacement meter to determine fractal dimension.

These techniques used are contact techniques. In these techniques tip deflection is used as a feedback signal. Because the measurement of a signal is prone to noise and drift, low stiffness cantilevers are used to amplify the deflection signal. However, close to the surface of the sample, attractive forces can be quite strong, causing the tip to "snap-in" to the surface. In order to avoid this we can use image processing techniques where there is no contact.

II. METHODOLOGY

In present study, the SEM image of the ductile and brittle fracture mode of fractured SS304 generated by [7] is considered. Images are of the 900 pixels in width and 900 pixels in height as shown in Figure.4 and Figure.5 respectively. Using the image processing techniques like Autosignal and Fractalyse the variation of fractal dimension is calculated in pixel count of 50pixels in both X and Y directions respectively.

2.1 Autosignal:

Fractal dimension calculation here is based on grey scale. Reference [8] found that fractal dimension depends on the grey scale and is same for 64 and 128 grey scale. The SEM images are used to generate 256 grey scale using Matlab and a [900x900] gray scale matrix is generated. Gray scale has values ranging from 0 to 255 where 0 stands for black color and 255 stands for white color. Gray scale matrix [900x900] generated is input for the Autosignal and by giving gray scale values from [50x900] matrix to [900x900] matrix in the intervals of 50 in horizontal and vertical direction respectively, Hurst exponent is estimated.

For calculation of fractal dimension using Hurst exponent for given gray scale matrix is suggested by [9] where (X_1,Y_1) to (X_n,Y_n) are gray scale matrix values for n pixel count. The sequence is

1. Calculate the mean;
   $m=1/n \sum_{i=1}^{n} X_i$
2. Create a mean-adjusted series;
   $Y_l = X_l - m$ for l=1, 2…, n.
3. Calculate the cumulative deviate series Z;
   $Z_l=\sum_{i=1}^{l} Y_i$ *for l=1, 2…, n.*
4. Compute the range R;
   R (n) = max (Z_1, Z_2 …, Z_n)-min (Z_1, Z_2 ..., Z_n)
5. Compute the standard deviation S;
   $S(n) = \sqrt{\frac{1}{n}\sum_{i=1}^{n}(X_i - m)^2}$
6. Calculate the rescaled range R (n) / S (n) and average over all the partial time series of length n.
7. The Hurst exponent is estimated by fitting the power law $\frac{R(n)}{S(n)} = n^{H}$ to the data.
8. Fractal dimension is 1/H.

2.2 Fractalyse:

Fractal dimension is calculation is based on area-perimeter method. It is the most stable and least ambiguous method [10]. It can be used to determine the fractal dimension of linear features [11]. The area of a given feature will not change much when measured from the sources of different scales, but the perimeter measurements can change significantly. The fractal dimension obtained from an area-perimeter analysis to agree with the dimension obtained from a spectra analysis [1].

The SEM images are inputs to this image processing technique. By increasing the rectangular selection window from (50x900) pixels to (900x900) pixels in the increments of 50pixels, fractal dimension is calculated both in horizontal and vertical direction respectively.

III. RESULTS AND CONCULSIONS

In this study, variation of fractal dimension in horizontal and vertical direction in the intervals of 50 pixel count is shown in Figure. 6 and Figure. 7 respectively. Maximum and minimum fractal dimension is determined in the ductile and brittle fracture mode is tabulated in Table II. Ductile mode has fractal dimension range from 1.23-1.50 and brittle mode has fractal dimension range from 1.52-1.72.

TABLE II. Maximum and minimum fractal dimension in ductile and brittle mode (*a=Autosignal, b=Fractalyse)*

Fracture Mode	Fractal Dimension	X-direction		Y-direction	
		a.	*b.*	*a.*	*b.*
Ductile	D_{max}	1.50	1.48	1.38	1.35
	D_{min}	1.31	1.29	1.23	1.25
Brittle	D_{max}	1.69	1.63	1.72	1.70
	D_{min}	1.52	1.53	1.52	1.53

The range of fractal dimension found by these image processing techniques are convincing to the fractal dimension obtained by contact methods used.

ACKNOWLEDGMENT

The comments of an anonymous reviewer are gratefully acknowledged.

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Fig. 1 : Koch flake

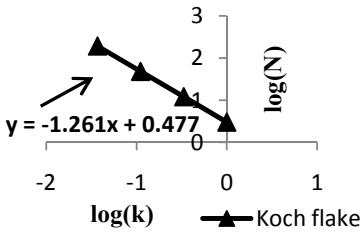

Fig. 2 : Fractal dimension determination of Koch flake

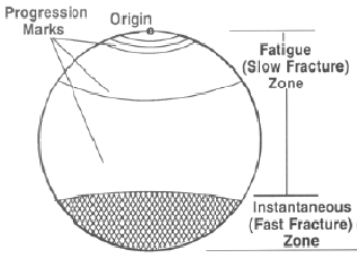

Fig. 3 : Macroscopic surface features (N.W.Sachs, 2005)

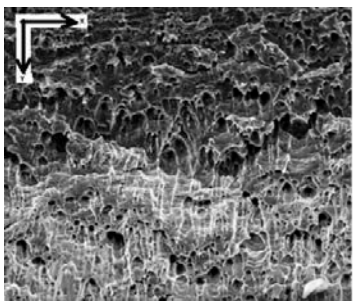

Fig. 4 : Ductile fracture mode observed(x500)

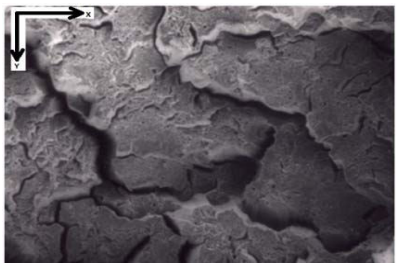

Fig. 5 : Brittle fracture mode observed(x500)

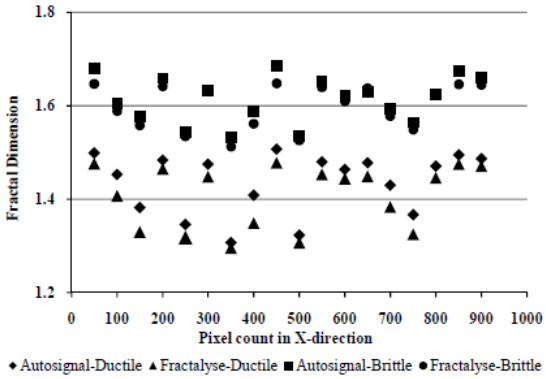

Fig. 6 : Variation of fractal dimension with pixel count in X-direction

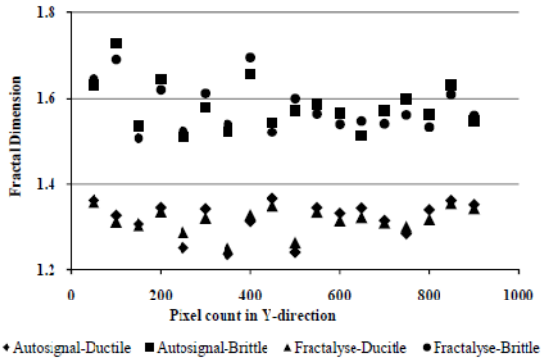

Fig. 7 : Variation of fractal dimension with pixel count in Y-direction

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Analysis of Two Level Voltage Source Inverter Using Space Vector Modulation

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Abstract - This paper presents (SVPWM) Space vector pulse width modulation technique of determining the switching sequence of upper three power transistor of a three phase voltage source inverter (VSI) fed 3ph induction motor drive. Space Vector is the best modulation technique to drive 3-phase load such as 3-ph Induction motor. In this paper the pulse width strategy with SVM analyzed in detail. The modulation Strategy uses the switching time calculator to calculate the timing of the voltage vector applied to the 3-ph balanced load. The principle of Space Vector Modulation is performed using MATLAB/SIMULINK. The simulation results indicate that this algorithm is flexible and suitable to use for advance Vector control. The strategy of switching minimizes the distortion of the load current as well as the loss due to minimize number of commutations in the inverter.

Keywords - *Harmonic Distortion, Space Vector Modulation, Inverter.*

I. INTRODUCTION

Recently, Due to growing of fast processor, many researches today show a great interest to develop a new or modify a PWM control algorithm to obtain good performances of AC drives. Developments in power electronics and semiconductor technology have lead improvements in power electronic systems. The induction motor (IM) thanks to its well known advantages of simple construction, reliability, ruggedness, and low cost has found very wide industrial applications. These advantages are superseded by control problems when using an IM in industrial drives with high Performance demands. Space vector PWM (SVPWM) technique is one of the most popular techniques gained interest recently. This technique results in higher magnitude of fundamental output voltage available as compared to sinusoidal PWM. This algorithm gives 15% more voltage output compare to the sinusoidal PWM algorithm thereby increasing the utilization of DC bus voltage. Furthermore it minimizes the T.H.D.[5]

II. PRINCIPLE OF SVPWM [1]

The circuit model of a typical three-phase voltage source PWM inverter is shown in Fig. 1. S1 to S6 are the six power switches that shape the output, which are controlled by the switching Variables a, a′, b, b′, c and c′. When an upper transistor is switched on, i.e., when a, b or c is 1, the corresponding lower transistor is switched off, i.e., the corresponding a′, b′c′ is 0.Therefore, the on and off states of the upper transistors S1, S3 and S5 can be used to determine the output voltage.

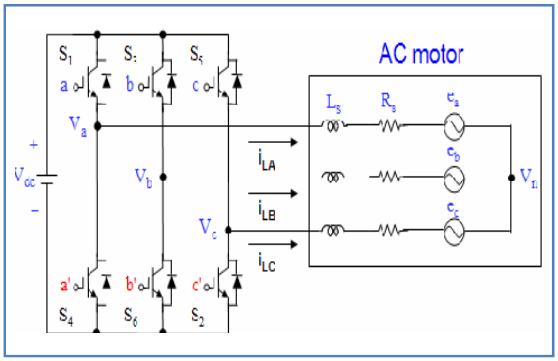


Fig. 1

The relationship between the switching variable vector [a, b, c]t and the line-to-line voltage Vector [Vab Vbc Vca]t is given by in the following:

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = V_{dc} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix}.$$

Also, the relationship between the switching variable vector [a, b, c]t and the phase voltage vector [Va Vb Vc]t can be expressed below.

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{V_{dc}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix}.$$

Voltage Vectors	Switching Vectors			Line to neutral voltage			Line to line voltage		
	a	b	c	V_{an}	V_{bn}	V_{cn}	V_{ab}	V_{bc}	V_{ca}
V_0	0	0	0	0	0	0	0	0	0
V_1	1	0	0	2/3	-1/3	-1/3	1	0	-1
V_2	1	1	0	1/3	1/3	-2/3	0	1	-1
V_3	0	1	0	-1/3	2/3	-1/3	-1	1	0
V_4	0	1	1	-2/3	1/3	1/3	-1	0	1
V_5	0	0	1	-1/3	-1/3	2/3	0	-1	1
V_6	1	0	1	1/3	-2/3	1/3	1	-1	0
V_7	1	1	1	0	0	0	0	0	0

(Note that the respective voltage should be multiplied by V_{dc})

Table 1 : Switching vectors, phase voltages and output line to line voltages.

Space Vector PWM (SVPWM) refers to a special switching sequence of the upper three power transistors of a three-phase power inverter. It has been shown to generate less harmonic distortion in the output voltages and or currents applied to the phases of an AC motor and to provide more efficient use of supply voltage compared with sinusoidal modulation technique as shown in Fig.2.

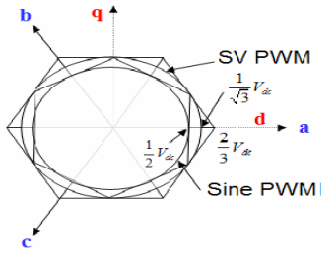


Fig. 2 : Locus comparison of maximum linear control voltage in Sine PWM and SVPWM.

To implement the space vector PWM, the voltage equations in the *abc* reference frame can be transformed into the stationary *dq* reference frame that consists of the horizontal (d) and vertical (q) axes as depicted in Fig.

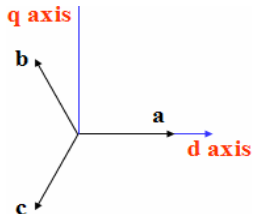


Fig. 3 : The relationship of abc reference frame and stationary dq reference frame

From this figure, the relation between these two reference frames is below

$$\mathbf{f}dq0 = \mathbf{K}s\mathbf{f}abc$$

This transformation is equivalent to an orthogonal projection of [a, b,c]t into the two-dimensional perpendicular to the vector [1, 1, 1]t (the equivalent d-q plane) in at three-dimensional coordinate system. As a result, six non-zero vectors and two zero vectors are possible. Six nonzero vectors (V1 - V6) shape the axes of a hexagonal as depicted in Fig. 3, and feed electric power to the load. The angle between any adjacent two non-zero vectors is 60degrees. Meanwhile, two zero vectors (V0 and V7) are at the origin and apply zero voltage to the load. The eight vectors are called the basic space vectors and are denoted by V0, V1, V2, V3, V4, V5, V6, and V7.

The same transformation can be applied to the desired output voltage to get the desired reference voltage vector Vref in the d-q plane.

The objective of space vector PWM technique is to approximate the reference voltage vector Vref using the eight switching patterns. One simple method of approximation is to generate the average output of the inverter in a small period, T to be the same as that of Vref in the same period.

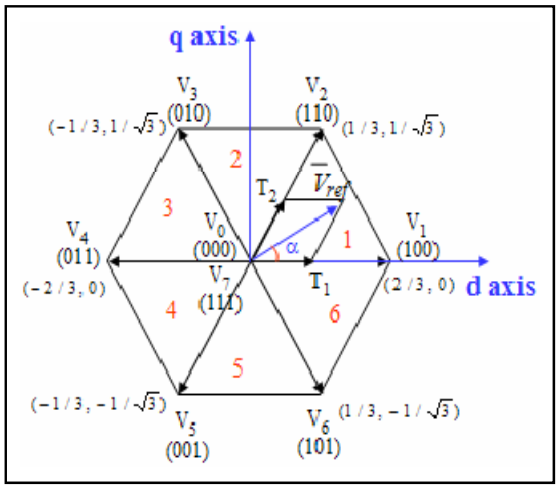


Fig. 4 : Basic switching vectors and sectors

Therefore, space vector PWM can be implemented by the following steps:

Step 1. Determine Vd, Vq, Vref, and angle (α)

Step 2. Determine time duration T1, T2, T0

Step 3. Determine the switching time of each transistor (S1 to S6)

Step 1: Determine Vd, Vq, Vref, and angle (α)

From Fig. , the Vd, Vq, Vref, and angle (α) can be determined as follows

$$V_d = V_{an} - V_{bn} \cdot \cos 60 - V_{cn} \cdot \cos 60$$
$$= V_{an} - \frac{1}{2} V_{bn} - \frac{1}{2} V_{cn}$$
$$V_q = 0 + V_{bn} \cdot \cos 30 - V_{cn} \cdot \cos 30$$
$$= V_{an} + \frac{\sqrt{3}}{2} V_{bn} - \frac{\sqrt{3}}{2} V_{cn}$$

IVrefI=√Vd2+Vq2

α= atan (Vq/ Vd)=wt=2*pi*f

Where, f=fundamental frequency

Step 2: Determine time duration T1, T2, T0

$$\int_0^{T_z} \overline{V}_{ref} = \int_0^{T_1} \overline{V}_1 dt + \int_{T1}^{T_1+T_2} \overline{V}_2 dt + \int_{T_1+T_2}^{T_z} \overline{V}_0$$

$$\therefore T_z \cdot \overline{V}_{ref} = (T_1 \cdot \overline{V}_1 + T_2 \cdot \overline{V}_2)$$

$$\Rightarrow T_z \cdot |\overline{V}_{ref}| \cdot \begin{bmatrix} \cos(\alpha) \\ \sin(\alpha) \end{bmatrix} = T_1 \cdot \frac{2}{3} \cdot V_{dc} \cdot \begin{bmatrix} 1 \\ 0 \end{bmatrix} + T_2 \cdot \frac{2}{3} \cdot V_{dc} \cdot \begin{bmatrix} \cos(\pi/3) \\ \sin(\pi/3) \end{bmatrix}$$

(where, $0 \le \alpha \le 60°$)

$$\therefore T_1 = T_z \cdot a \cdot \frac{\sin(\pi/3 - \alpha)}{\sin(\pi/3)}$$

$$\therefore T_2 = T_z \cdot a \cdot \frac{\sin(\alpha)}{\sin(\pi/3)}$$

$$\therefore T_0 = T_z - (T_1 + T_2), \quad \left(\text{where,} \quad T_z = \frac{1}{f_z} \quad \text{and} \quad a = \frac{|\overline{V}_{ref}|}{\frac{2}{3} V_{dc}} \right)$$

- Switching time duration at any Sector

$$\therefore T_1 = \frac{\sqrt{3} \cdot T_z \cdot |\overline{V}ref|}{V_{dc}} \left(\sin\left(\frac{\pi}{3} - \alpha + \frac{n-1}{3} \pi \right) \right)$$
$$= \frac{\sqrt{3} \cdot T_z \cdot |\overline{V}ref|}{V_{dc}} \left(\sin \frac{n}{3} \pi - \alpha \right)$$
$$= \frac{\sqrt{3} \cdot T_z \cdot |\overline{V}ref|}{V_{dc}} \left(\sin \frac{n}{3} \pi \cos\alpha - \cos \frac{n}{3} \pi \sin\alpha \right)$$

$$\therefore T_2 = \frac{\sqrt{3} \cdot T_z \cdot |\overline{V}ref|}{V_{dc}} \left(\sin\left(\alpha - \frac{n-1}{3} \pi \right) \right)$$
$$= \frac{\sqrt{3} \cdot T_z |\overline{V}ref|}{V_{dc}} \left(-\cos\alpha \cdot \sin \frac{n-1}{3} \pi + \sin\alpha \cdot \cos \frac{n-1}{3} \pi \right)$$

$$\therefore T_0 = T_z - T_1 - T_2, \quad \left(\begin{matrix} \text{where, n = 1 through 6 (that is, Sector1 to 6)} \\ 0 \le \alpha \le 60° \end{matrix} \right)$$

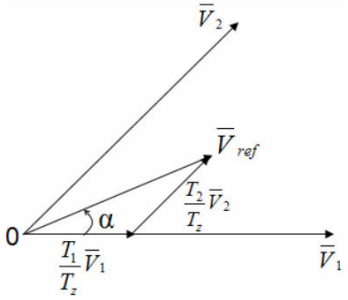
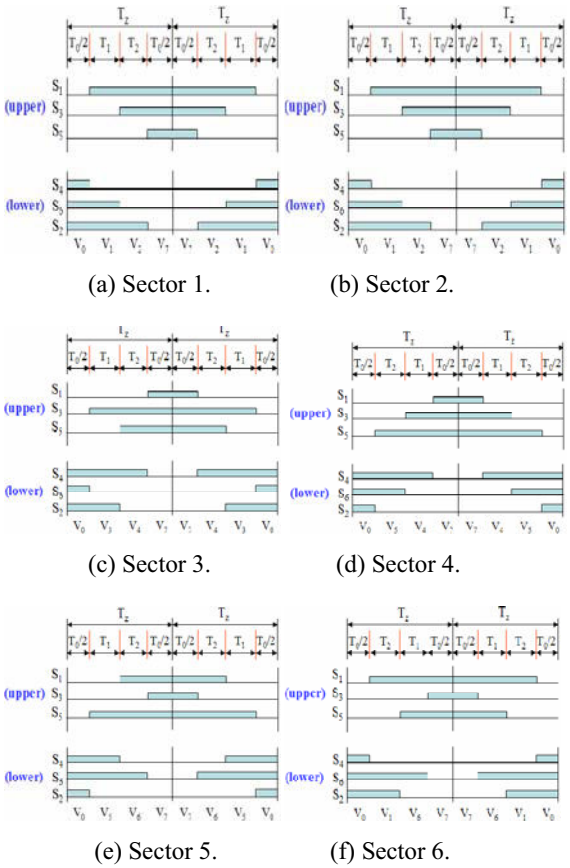


Fig. 5 : Reference vector as a combination of adjacent vectors at sector 1.

Step 3: Determine the switching time of each transistor (S1 to S6)

Fig. 6 shows space vector PWM switching patterns at each sector.



(a) Sector 1. (b) Sector 2.

(c) Sector 3. (d) Sector 4.

(e) Sector 5. (f) Sector 6.

Fig. 6 : Space Vector PWM switching patterns at each sector

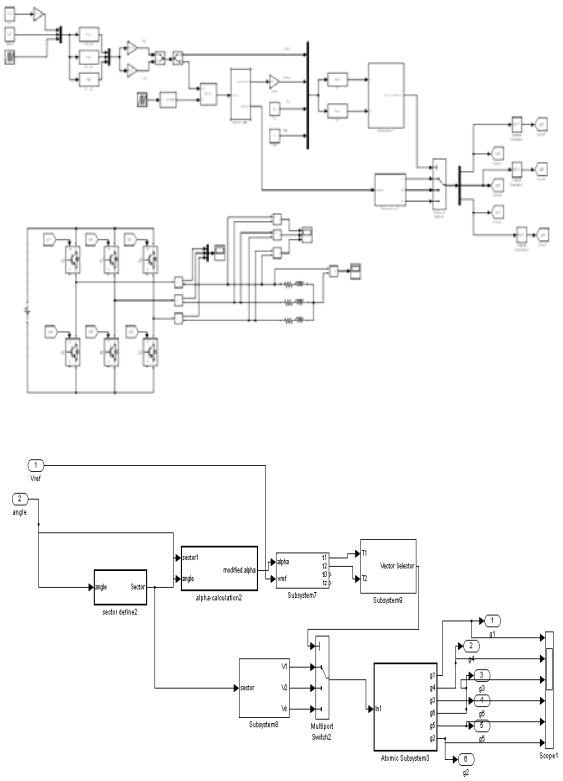
Space Vector PWM switching patterns at each Based on Fig. the switching time at each sector is summarized in Table 2, and it will be built in Simulink model to implement SVPWM.

sector.

Sector	Upper Switches (S_1, S_3, S_5)	Lower Switches (S_4, S_6, S_2)
1	$S_1 = T_1 + T_2 + T_0/2$ $S_3 = T_2 + T_0/2$ $S_5 = T_0/2$	$S_4 = T_0/2$ $S_6 = T_1 + T_0/2$ $S_2 = T_1+T_2+T_0/2$
2	$S_1 = T_1 + T_0/2$ $S_3 = T_1 + T_2 + T_0/2$ $S_5 = T_0/2$	$S_4 = T_2 + T_0/2$ $S_6 = T_0/2$ $S_2 = T_1+T_2+T_0/2$
3	$S_1 = T_0/2$ $S_3 = T_1 + T_2 + T_0/2$ $S_5 = T_2 + T_0/2$	$S_4 = T_1+T_2+T_0/2$ $S_6 = T_0/2$ $S_2 = T_1 + T_0/2$
4	$S_1 = T_0/2$ $S_3 = T_1 + T_0/2$ $S_5 = T_1 + T_2 + T_0/2$	$S_4 = T_1+T_2+T_0/2$ $S_6 = T_2 + T_0/2$ $S_2 = T_0/2$
5	$S_1 = T_2 + T_0/2$ $S_3 = T_0/2$ $S_5 = T_1 + T_2 + T_0/2$	$S_4 = T_1 + T_0/2$ $S_6 = T_1+T_2+T_0/2$ $S_2 = T_0/2$
6	$S_1 = T_1 + T_2 + T_0/2$ $S_3 = T_0/2$ $S_5 = T_1 + T_0/2$	$S_4 = T_0/2$ $S_6 = T_1+T_2+T_0/2$ $S_2 = T_2 + T_0/2$

Table 2 : Switching Time Calculation at Each Sector

IV. SIMULATION RESULTS



Simulation models of two-level inverter

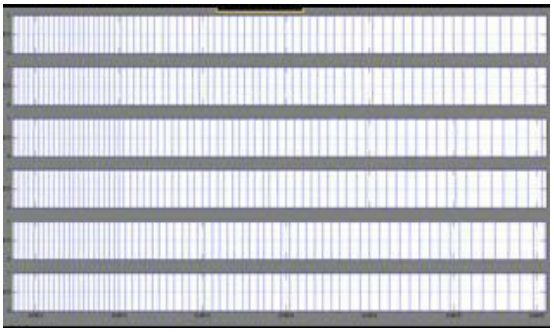


Fig. 7 : Gate pwm pulses for six switches.

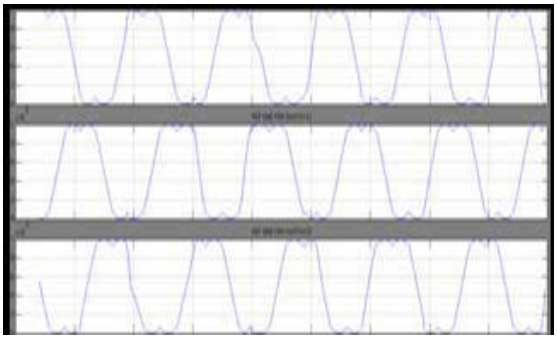


Fig. 8 : Ref voltage for upper three switches which Remove third harmonics.

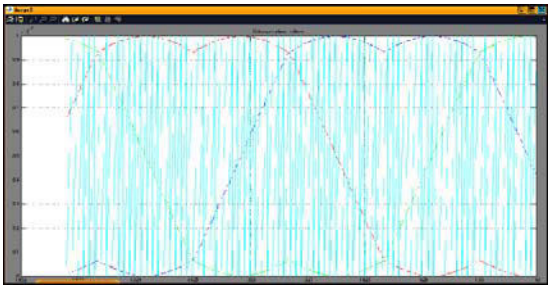
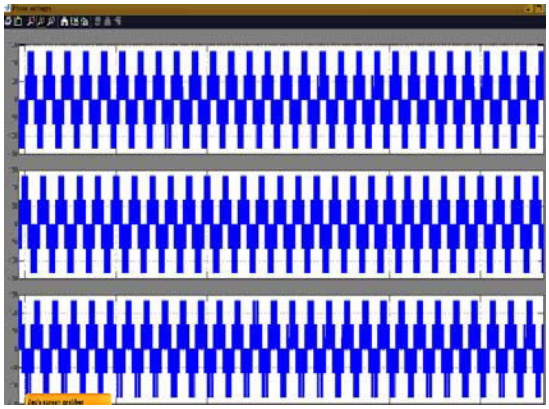


Fig. 9 : Ref voltages compared with Carrier

Fig. 10 : Waveform of three line-to line voltage-(stator voltages)



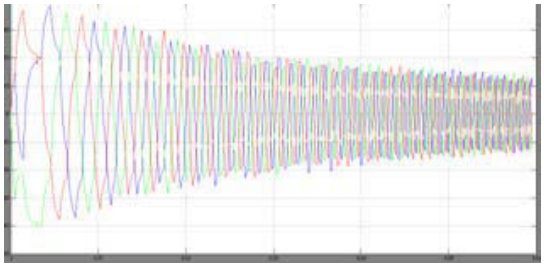


Fig. 11 : waveforms of stator currents

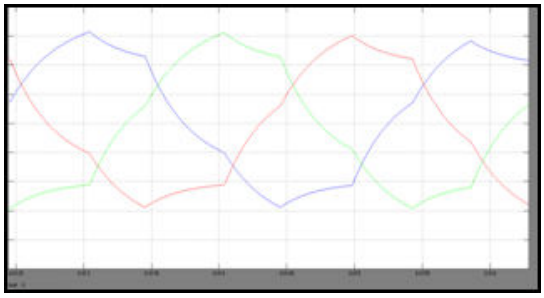


Fig. 12 : Waveform of stator currents

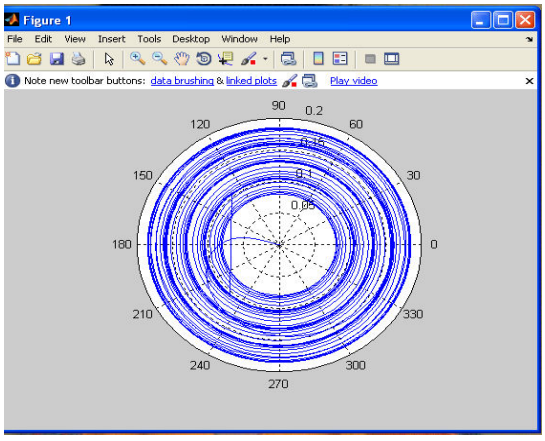


Fig.13 : Polar plot of Vref and angle theta

Appendix:

Motor data and parameters:

220V,3-phase,2 pole,1 HP, 50Hz

Rs=9.6 ohm, Ls=0.8896 H

Rr=7.08 ohm, Lr= 0.9996 H

Tz=1 khz

V. CONCLUSION:

Space Vector Modulation technique only requires a one reference space vector to generate 3-ph sine waves. The amplitude and load voltage can be varied by controlling the reference space vector. This algorithm is very popular in ac drive applications. Furthermore this algorithm is flexible and suitable for advance control of ac drives. It also minimizes the distortion in the load current. As shown in the simulation results (fig 8) that there are ref voltages having no tripllen harmonics so this leads to higher modulation index compared to SVPWM.[5]

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Diminished-1 Modulo 2^n+1 RNS Adder with Embedded Reverse Converter

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Abstract - A RNS adder is integral part of any DSP based system which works on Residue Number System (RNS). In this paper we have presented an area efficient version of the Diminished-1modulo 2^n+1 RNS adder, which employs diminished-1 representation of numbers to enable easier and faster computation. We have designed a reverse converter to convert back the RNS sum to binary format, which has been embedded with the adder module so that it can act as a stand - alone unit. The entire unit has been developed and tested in VHDL environment, the RNS adder unit has been mapped to TSMC 130 nm implementation technology using Synopsys Design Compiler. The area and power consumed by the design have been recorded from the above tool for various of n= 8, 16, 32,64,128,256.

Keywords - VLSI Design, Residue Number System (RNS), Diminished-1, Circular Carry Select (CCS).

I. INTRODUCTION

Residue Number System (RNS) has been creating a lot of interest as it evolves to be an imminent aspect of fast computational hardware [1]. This has led to intense concentration of RNS in areas of Arithmetic Computation, Signal Processing Applications, Image Processing, FFT, Digital Frequency Synthesis, Video Filters, 2-D filters, NTTs (Number Theoretic Transforms), Cryptography [2],[3]. RNS is a non-weighted number system, based on congruence relation. The main features of RNS are parallelism, modularity, and fault tolerant and parallel carry- free operation [4]. The main aspects of RNS are selection of moduli and reverse conversion of residues back to the desired radix representation.

The moduli selection in RNS is crucial part which is based on the set of moduli $\{2^n\text{-}1, 2^n, 2^n\text{+}1\}$ of which 2^n+1 has gained most popularity due to its reduced area and delay characteristics. In the proposed design a 2^n+1 is a fundamental part of the 4 – moduli RNS adder [6]. Modulo 2^n+1 channel has the ability to handle n+ 1 bit, whereas other moduli sets can handle only n bits.

Diminished-1 number representation [7] proposed by Leibowitz has been implemented in modulo 2^n+1 RNS adder that makes the adder unit more versatile in terms of area and power consumed by the entire circuit. Diminished- 1representation has n+ 1 bit to represent a number, which enables to represent zero in a unique mode that enables to save valuable resources in the design.

Reverse conversion of RNS to binary representation is based on the Chinese Remainder Theorem (CRT), widely used as a standard method for the RNS reverse conversion. We have an assumed a most widely used moduli set of $\{2^n\text{-}1, 2^n, 2^n\text{+}1\}$ in our computation process. The dynamic range is constant for a given values of moduli in an operation. Reverse Conversion methodology is briefly explained in the works [10], [11] that gives an account of efficient design of the converter for the moduli set we work on. The term RNS adder unit critically refers to the combined unit of RNS adder and Reverse Converter module together.

This work describes a Diminished-1 modulo 2^n+1 RNS adder that performs RNS addition between two values in Diminished-1 domain. The RNS sum thus obtained from the proposed unit has to be converted into binary format to be used in the system for further process; we have developed a reverse converter to attain this objective. The computation operation in Diminished-1 representation facilitates us to have less area and power consumed by the overall design that has been illustrated in the paper.

The paper presents itself with the facts of Diminished-1 modulo 2^n+1 RNS adder unit are described in section I, performance parameters and comparisons are presented in section II, followed by conclusion in section III.

II. DIMINISHED-1 MODULO 2^n+1 RNS ADDER UNIT

RNS is defined by a set of co – prime integers, $(m_1,m_2,m_3,\ldots,m_n)$ termed as moduli, a given integer q can be converted into residue representation by $(q_1,q_2,q_3,\ldots.q_n)$ are the least possible positive remainders of the integer q when divided by the set of moduli

$(m_1,m_2,m_3,\ldots,m_n)$ [4]. It is indicated by $r_i=|q|m_i$, where r is the residue of the integer for the particular moduli, this procedure has to be followed on the specific integer for all values of moduli to have the residue representation of the integer q.

The residues can be operated upon to get the desired arithmetic function on the numbers. Now we represent the obtained residues of the integers in the diminished-1 representation. In diminished-1 representation a number q is given as a $q^{\#} = q - 1$. All possible residues of an integer so obtained from the moduli are converted into the diminished-1 format. In this representation of numbers zero representation only holds a special citation, as it is the only entity to be given with the msb being 1 and all other bits as 0. If n = 4 then 0 is given as 10000 [7]. So when we encounter zero in any one of the residues then we can take the other residue as the result, since 0 doesn't affect the result of the addition process. This enables us to save time and area in the design of the circuit.

For any two integers q and p to be in RNS format p = $(p_1, p_2, p_3 \ldots p_n)$, and q = $(q_1, q2, q3 \ldots qn)$, theses residues are then transformed into their diminished-1 equivalents to be taken into further steps of the function. $(p_1^{\#}, p_2^{\#}, p_3^{\#}, \ldots, p_n^{\#})$ and $(q_1^{\#},q_2^{\#},q_3^{\#},\ldots,q_n^{\#})$ would be the residues available for the addition process.

$(s_1,s_2,\ldots,s_n) = (p_1^{\#}, p_2^{\#}, p_3^{\#} \ldots p_n^{\#}) + (q_1^{\#},q_2^{\#},q_3^{\#},\ldots,q_n^{\#})$

The result gives us the process gives us the required result in the RNS format, which can be converted back to the required radix by the reverse conversion process of the residue number system [8], [9]. The reverse conversion is the most important aspect of the RNS number system so it is mainly based on the Chinese Remainder Theorem (CRT)

$$x = \sum_{i=1}^{N} A_i T_i r_i mod\ m$$

Dynamic range is the product of all the moduli we use in a particular computation. A_i is given by ratio of dynamic range to the moduli (m_i). T_i is the multiplicative inverse of the moduli and A_i which is obtained using Euclid's theorem. r_i is the sum we obtained from adder unit for a moduli m_i. The sum of this for all values of moduli gives the resultant value in Mixed Radix Representation [2]. The reverse converter in the design has been designed in the lines of the reverse conversion methodology mentioned here.

The conversion methodology used in the design is simple for a 4 moduli set computation process,

III. PERFORMANCE EVALUATION

The Diminished-1 modulo 2^n+1 RNS adder unit has been developed and simulated using VHDL codes and has been mapped to 130 nm using Synopsys Design Compiler for n = 8, 16, 32,64,128,256. The codes for the design have been developed using hybrid modeling of VHDL. The area and power values for various values of n calculated by Synopsys Design Compiler have been presented in the Table 1.

TABLE I
Performance parameters of proposed Diminished-1 modulo 2^n+1 RNS adder

N	Module	Area (μm^2)	Power (mW)
8	RNS Adder	552	0.00104
	Reverse Converter	55173	0.38
16	RNS Adder	1056	0.00223
	Reverse Converter	60441	0.417
32	RNS Adder	2124	0.00840
	Reverse Converter	63912	0.471
64	RNS Adder	3768	0.0109
	Reverse Converter	63912	0.471
128	RNS Adder	6916	0.0170
	Reverse Converter	63912	0.471
256	RNS Adder	13328	0.0273
	Reverse Converter	63912	0.471

IV. CONCLUSION

In this paper, we have implemented a diminished – 1 Modulo 2n+1 RNS Adder embedded with a reverse converter module. The entire operation of RNS addition takes place in the adder unit and sum which in the RNS domain is converted back to binary format with the help of the reverse converter for the given 4 moduli set. The performance parameters of the design like the area and power values for values of n = 8, 16, 32, 64, 128, 256 are given here in Table.1.

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SECTION-III

Artificial Intelligence and Soft Computing

Development of Artificial Neural Network (ANN) based Prediction Model for NOx Emissions from Utility Boilers

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Abstract **-** NOx emissions are measured in the effluent gas from utility boilers. These emissions are controlled by a variety of different features during combustion or post combustion. Firstly all the 15 different features affecting NOx emissions from utility boilers, directly or indirectly were identified. Dominant features are selected based on their importance through sound statistics approach using F-distribution and its corresponding p-value. In this paper, The NOx emission prediction is done based on the 10 dominant features selected using Artificial Neural Network model called General Regression Neural Network. In this model the smoothing factor is generated using a Genetic Algorithm. Finally an Artificial Neural Network prediction tool has been generated with Visual Basic front-end to predict the NOx in utility boilers

Keywords- *NOx, Emissions, Feature Selection, F-distribution, Prediction, Artificial Neural Network, General Regression Neural Network, Smoothing Factor, Genetic Algorithm*

I. INTRODUCTION

With increased environmental regulations both in the developed and developing world, the onus lies on us to reduce NOx emissions from utility boilers. NOx emissions are one of the most toxic forms of pollutants that harm the environment and the ecosystem surrounding us. NOx can be controlled in two phases: during combustion; post combustion. Combustion controls could include flue gas recirculation, over fire air, low NOx burners and reburn. Post combustion controls could include Selective Non-Catalytic Reduction (SNCR) or Selective Catalytic Reduction (SCR) [1]. Alternative techniques for reducing NOx could be practiced like Burner Out Of Service (BOOS), wherein fuel flow is stopped from individual burners and air flow is maintained through idle burners or Biased Firing (BF) wherein more fuel is injected to some burners and amount of fuel is reduced to other burners.

Even with all this knowledge, NOx emission phenomena is understood to a little extent. More and more studies have to be conducted on the subject and model understanding has to improve. In this paper we are attempting to generate an Artificial Neural Network (ANN) prediction model for NOx emissions from utility boilers resulting in a prediction tool.

Due to lack of sound model understanding of the NOx emission prediction phenomena, we have to first identify all or few dominant features that affect NOx emission. As a result of this exercise we have identified, C%, H%, N%, O%, total air flow, excess air, mill combination, burner tilt, load, no. of mills, coal gross calorific value (gcv), total coal flow, capacity load, volatile matter, ash and moisture. Mill combination and no. of mills fired were combined into a single input by arranging the mill combination in 10 bit pattern and setting the bit to 1 if mill is fired otherwise setting the bit to 0 if mill is not fired. Final mill combination input was taken as the decimal value corresponding to the 10 bit binary pattern.

Once feature selection was broadly done an exercise to identify dominant features affecting NOx emissions was carried out. This exercise uses F-distribution and its corresponding p-value as the basis.

Around 50 field data consisting of NOx with few required influencing features were taken and analyzed using General Regression Neural Network (GRNN). The smoothing factor for the GRNN was generated by a Genetic Algorithm. A visual basic front-end interface was created which was dynamically linked to a Definition file and a Dynamic Linked Library (DLL) file. On entering data to the front-end menu and firing the neural network predicted NOx is seen as a separate field in the menu.

II. METHODOLOGY FOR FEATURE SELECTION

Feature Selection in Artificial Neural Networks may be done using weight pruning [2], the first order derivative of the output and the second order derivative of the output or may be extracted using statistical methods like principal component analysis and independent component analysis [3]. But using F-distribution and its corresponding p-value apparently seems to be the most appropriate feature selection technique especially to select the dominant features.

In this paper F-distribution and its corresponding p-value have been used to short-list 10 dominant features that are fed in as input to the GRNN. F-distribution is an asymmetric distribution which compares the variances of two distributions and lower the p value the hypothesis is significant and true. Feature selection can be done based on the comparison of variances of respective distributions and 10 dominant features are selected from the 15 features extracted. This is a case of dimensionality reduction and is useful in focusing the GRNN to train better and give a better prediction of the NOx output. This is illustrated in Figure 1 and Table 1.

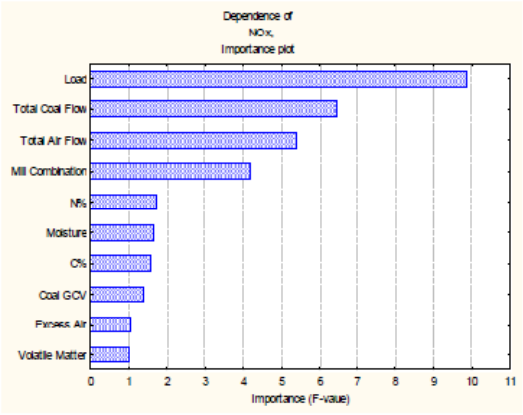

Figure 1: Feature Selection based on 10 best predictors

Feature	F - Value	p - Value
Load	9.855183	0.000001
Total Coal Flow	6.461709	0.000037
Total Air Flow	5.402300	0.000328
Mill Combination	4.180889	0.005900
N%	1.719806	0.123619
Moisture	1.669696	0.143649
C%	1.567427	0.165534
Coal GCV	1.394487	0.228617
Excess Air	1.033853	0.417186
Volatile Matter	1.008008	0.320522

Table 1: Indicates Feature with corresponding F and p value

III. NOX PREDICTION USING GRNN

The 10 dominant features as listed above have been taken as input to the neural network. The neural network model chosen for analysis is General Regression Neural Networks (GRNN). The GRNN model comprises of the feature to be predicted called the dependent variable and all the features on which the prediction depends on called the predictor variables. The GRNN predicts the dependent variable that varies continuously as output. The method of regression involves minimizing the square of the difference between actual and predicted values. This is called method of least squares [4].

The essence of the GRNN model lies in identifying a smoothing factor. In the present case, the smoothing factor is generated by a Genetic Algorithm. The smoothing factor determines the nearness of fit of the neural network predicted value to the actual value. This is done by regression and measurement of Euclidean distance between actual and predicted values. If the smoothing factor is too large it will result in small resolution. If the smoothing factor is too small it will result in large statistical variability [4]. The actual and predicted NOx from the GRNN output is shown in Figure 2 with the results being summarized in Table 2.

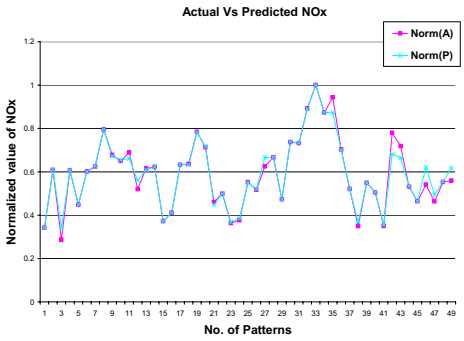

Figure 2: Figure showing Actual Vs. Predicted NOx

Network type	GRNN, genetic adaptive
Patterns processed	49
Smoothing factor	0.1342353
Output	NOx (in ppm)
R squared	0.9718
r squared	0.9739
Correlation Coefficient r	0.9868
Mean Absolute Error	6.557

Table 2: Indicates results of the trained GRNN

IV. INFERENCES BASED ON MODEL UNDERSTANDING

Considering NOx to be a fairly continuous output, GRNN model fits in very well. The correlation coefficient of 0.9868 is indicative of the accuracy of prediction [5].

V. NOX PREDICTION TOOL

A front-end was created in Visual Basic. This was dynamically linked to a DLL and a definition file generated from the neural network program [6]. The definition file carries all information of the trained neural network model. The DLL file is a pointer to all the required files that are needed for linking to the Visual Basic front-end. A program was written in Visual Basic that invoked the definition file, the DLL file, and the front-end form; screen-shot is given in Figure 3. The program triggers us to fire the trained neural network and gives NOx predictions accordingly after suitable interpolations. The exe file was bundled and packaged so that it could be setup on a remote machine.

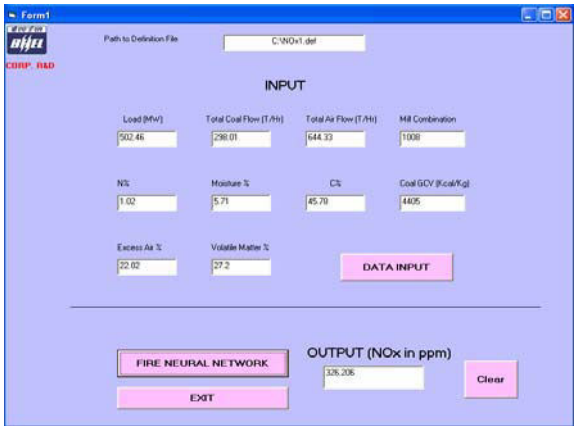

Figure 3: Screenshot of NOx Prediction Tool

VI. CONCLUSION

Feature Selection is an important aspect of neural network training. Once the 10 dominant features of the neural network were selected by F-distribution and its corresponding p-value, the results were fed into a GRNN and better prediction results were obtained.

A neural network prediction tool was also created with a front-end Visual Basic interface which could be set up on a remote machine after bundling the exe file with the definition file and DLL file.

ACKNOWLEDGMENT

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Development and Application of Artificial Neural Network model for Prediction of Surface Roughness

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Abstract - Monitoring of surface roughness of machined components is important measure of quality control. To assist this process an Artificial Neural Network based model for predicting the Surface Roughness is presented in this study. A Multilayer Perceptron (MLP) Neural Network is used to model and predict Surface Roughness value. Parameters like peak current, sparking gap, on time & duty cycle of Electro Discharge Machined (EDM) Surface is used as input data sets for training and testing ANN model. The results showed that ANN predicted Surface Roughness values (ANN Ra) were found in good agreement with Experimental Ra value. Thus an ANN model of this kind can be combined with noncontact methods for online Surface Roughness Monitoring.

Keywords- *ANN, MLP, Surface Roughness (Ra), ANN Ra, Experimental Ra*

I. INTRODUCTION

An artificial neural network is a system based on the operation of biological neural networks, in other words, is an emulation of biological neural system. A neural network has to be configured such that the application of a set of inputs produces the desired set of outputs. Various methods to set the strengths of the connections exist. One way is to set the weights explicitly, using a priori knowledge. Another way is to train the neural network by feeding it teaching patterns and letting it change its weights according to some learning rule. The learning situations in neural networks may be classified into three distinct sorts. These are supervised learning, unsupervised learning, and reinforcement learning. In supervised learning, an input vector is presented at the inputs together with a set of desired responses, one for each node, at the output layer. A forward pass is done, and the errors or discrepancies between the desired and actual response for each node in the output layer are found. These are then used to determine weight changes in the net according to the prevailing learning rule. [1]

The term supervised originates from the fact that the desired signals on individual output nodes are provided by an external teacher. In unsupervised learning (or self-organization), a (output) unit is trained to respond to clusters of pattern within the input. Reinforcement learning is learning what to do – how to map situations to actions. The learner is not told which actions to take, as in most forms of machine learning, but instead must discover which actions yield the most reward by trying them.

A very important feature of these networks is their adaptive nature, where "learning by example" replaces "programming" in solving problems. This feature makes such computational models very appealing in application domains where one has little or incomplete understanding of the problem to be solved but where training data is readily available. A group of samples are used to train the neural network by providing it with a number of input-output process parameters value combinations. Hence, the network is learned with what may be the output for the given input value. [11].

II. ESTIMATION OF SURFACE ROUGHNESS PARAMETERS

The most important requirement in roughness assessment using Artificial Neural Network is to extract surface roughness features measured by Ra stylus and finding out the best ANN model for prediction of surface roughness values that can produce results for variety of values of input variables by the training, testing and evaluation of the network architectures of different structures. [6]

In this work, Surface Roughness features were extracted from Ra stylus results and the four input parameters peak current, sparking gap, on time and duty cycle were used to characterize the surface roughness of the EDM machined work piece. [8]

A. Surface Roughness

The four variable parameters (peak current, sparking gap, on time, duty cycle) were used as inputs, while the Surface Roughness was used as output parameter for the training and testing of the Artificial Neural Network model. The actual surface roughness

with which the ANN results are compared was measured by Ra stylus. **[7]**

Ra is the arithmetic average of the roughness profile. The roughness profile contains *n* ordered, equally spaced points along the trace, and y_i is the vertical distance from the mean line to the i^{th} data point. Height is assumed to be positive in the up direction, away from the bulk material. The average roughness, Ra, is expressed in units of height. The formula for the Surface Roughness Ra calculation is given by:

Arithmetic average Ra,

$$R_a = \frac{1}{n} \sum_{i=1}^{n} y\,i \qquad (1)$$

III. DEVELOPMENT OF NEURAL NETWORK MODEL

i) Design of the ANN model

Neural Network software Easy NN was used to design the neural network. The basic steps involved in designing the network were: Generation of data; Pre-processing of data; Design of the neural network elements; Training and testing of the neural network; Simulation and prediction with the neural networks; and Analysis and post-processing of predicted result. [4]

ii) Generation of dataset

In order to generate input/output dataset for training and testing of the network, a number of experimental results were used and the surface of EDM machined workpiece measured by stylus and analysed using the proposed ANN system.

iii) Pre-processing of data

The input/output dataset were normalized to range between 0 and 1 using the 'threading' function inbuilt with the Easy NN software. The dataset was then portioned randomly into two subsets: training dataset (75%), and testing dataset (25%). The target error was fixed to 0.01 and the learning rate was set to 0.6. The momentum was fixed as 0.8.

iv) Design of the Neural Network elements

Feed-forward Multilayer Perceptron (MLP) neural network [5] with 4 layers was finally designed, trained and tested after trial of number of architecture structures. There were four neurons in the input layer, three in the both hidden layer, while there was one neuron in the output layer. The structure of the neural network as developed in Easy NN software is shown in Figure-1. [11]

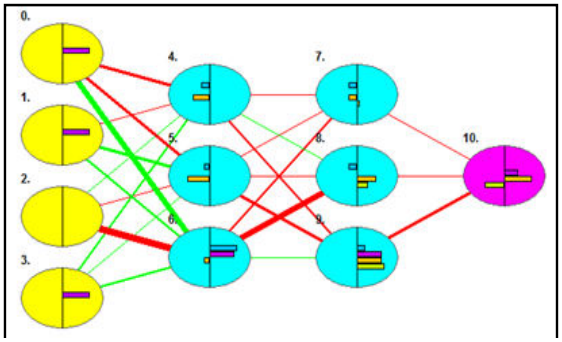

Fig.1.The model of feed-forward multilayer ANN used to predict surface roughness.

Table-1 ANN model specifications

Optimal ANN architecture and its specifications	
Neural Network	MLP
No. of hidden layers	2
No. of neurons in the input layer	4
No. of neurons in first hidden layer	3
No. of neurons in second hidden layer	3
No. of neurons in output layer	1
Learning rate	0.6
No. of learning cycles	100
Target error	0.01
Momentum	0.8

v) Training of the neural network

The training of the network was carried out by the inbuilt training algorithm in Easy NN software which is used because of its fast convergence and accuracy for training the network. The training is terminated automatically when the preset number of cycles 100 is finished and the average training is below the target error fixed as 0.01. [4]

vi) Testing of the ANN model

The testing of ANN model is carried out by analyzing the difference between predicted and the network training outputs. That difference was used for finding out the percentage validation error of the training phase. The predictive performance accuracy of the network was determined based on the coefficient of determination between the predicted and the experiment values of Surface Roughness of the EDM machined surface. [1]

IV . RESULTS AND DISCUSSION

In the present case, the training of various neural networks was carried out with different network architectures and finally a network which provides the

best results with minimum error is found out. The optimum model is thus finalised and fixed for the same type of data prediction, analysis and also for validating results obtained experimentally.

The comparison between the ANN predicted Surface Roughness values (ANN Ra) and Experimental Roughness (Ra) values are shown in figure-2. The result shows that the ANN model is able to predict the surface roughness with good accuracy.

The graph shows good agreement of the experimental Ra and the ANN predicted Ra values.

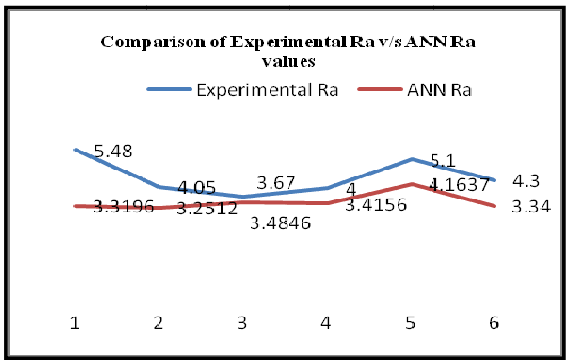

Fig. 2 Comparison of Actual Ra v/s ANN Ra

V. CONCLUSION

The Error Between The ANN Predicted Ra And The Experimental Ra Results As Shown In Figure-2 Are Within 20%. This Shows Good Agreement Of ANN Predicted Ra With Experimental Ra. The Deviation Can Be Further Reduced If The Training Dataset Values Are Increased. This Will Also Enhance The Accuracy Of The Existing ANN Model. Thus, We Can Conclude That The Prediction Of Value Of Surface Roughness Or Any Other Parameter Can Be Carried Out By Suitable Best ANN Model Within The Levels Of Input Parameters.

ACKNOWLEDGMENT

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Modeling of Internal Parameters for Supercapacitor Using Charging and Discharging Characteristics

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Abstract **-** A new technology, the supercapacitor, has emerged with the potential to enable major advances in energy storage. Supercapacitors are governed by the same fundamental equations as conventional capacitors, but utilize higher surface area electrodes and thinner dielectrics to achieve greater capacitances. This allows for energy densities greater than those of conventional capacitors and power densities greater than those of batteries. As a result, Supercapacitors may become an attractive power solution for an increasing number of applications. A simple resistive capacitive equivalent circuit is insufficient to characterize its terminal behavior. The equivalent model consists of three RC branches, one of them with a voltage dependent capacitor. A method to identify the circuit parameters is presented. Measurements of carbon-based supercapacitor for power applications are presented, analyzed, and the equivalent circuit response is compared with experimental results. This gives the behavior of the supercapacitor which will help in any particular application in power electronics.

Keywords- *Supercapacitor, Electrochemical double layer capacitor, charging and discharging of supercapacitor, MATLAB/SIMULINK.*

I. INTRODUCTION

Supercapacitor is also known as ultra capacitor, electro-chemical double layer capacitor. It utilizes the high surface area electrode materials and thin electrolytic dielectrics to achieve capacitances several orders of magnitude larger than conventional capacitors. Supercapacitor can store much more energy than conventional capacitors and offer much higher power density than batteries. Supercapacitor fills up the gap between the batteries and the conventional capacitor, allowing applications for various power and energy requirements. Supercapacitor works on the principle of double-layer capacitance at the electrode/electrolyte interface where electric charges are accumulated on the electrode surfaces and ions of opposite charge are arranged on the electrolyte side.

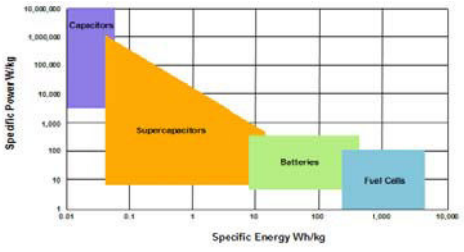


Fig.1: Rag one plot of various energy storage devices

Supercapacitor devices consist of two electrodes to allow a potential to be applied across the cell, and therefore double-layers present, one at each electrode/electrolyte interface. An ion-permeable separator is placed between the electrodes in order to prevent electrical contact, but still allows ions from the electrolyte to pass through it (Fig-1).

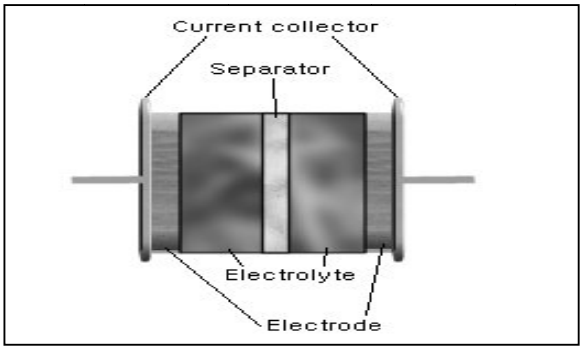


Fig.2:- Conceptual diagram of supercapacitor construction

The electrodes are made of high effective surface-area materials such as porous carbon, carbon aero gel or graphene in order to maximize the surface-area of the double layer. High energy densities are therefore achievable in supercapacitors due to their high specific capacitance, attained because of a high electrode/electrolyte interface surface area and a small charge layer separation of atomic dimensions. Polymer or paper separators can be used with organic electrolytes and ceramic or glass fiber separators are often used with aqueous electrolytes. For best supercapacitor

performance the separator should have a high electrical resistance, a high ionic conductance, and a low thickness.

Supercapacitors utilize an electrochemical double-layer of charge to store energy. As voltage is applied, charge accumulates on the electrode surfaces. Following the natural of unlike charges, ions in the electrolyte solution diffuse across the separator into the pores of the electrode of opposite charge. However, the electrodes are engineered prevent the recombination of the ions. Thus, a double-layer of charge is produced at each electrode. These double-layers, coupled with an increase in surface area and a decrease in the distance between electrodes, allow supercapacitors to achieve higher energy than conventional capacitors.

Because there is no transfer of charge between electrolyte and electrode, there are no chemical or composition changes associated with non-Faradic processes. For this reason, charge storage in supercapacitors is highly reversible, which allows them to achieve very high cycling stabilities.

II. PARAMETERS OF SUPERCAPACITOR

To study the internal parameter, behavior of supercapacitor is required. For this reason simple resistive capacitive model (series RC circuit) is used. In this paper carbon based supercapacitor is used. These capacitors are low voltage device with a rated voltage of 2.4 V with capacitance value of 540 F. Higher voltages can be achieved by connecting many cells in series like batteries. An equivalent circuit describes the terminal behavior of a supercapacitor.

In this paper the measured voltage of a 540 F supercapacitor charged up to the rated voltage with a constant current of 2 A**,** and discharged after some time with the same magnitude of constant current. It also shows the expected voltage, if the supercapacitor is described by a simple RC circuit. The noticeable differences between measured results and the simple model are the nonlinear rise and fall of the supercapacitor voltage and the change in voltage after the charging and discharging stops. This latter change cannot be explained by an internal discharge resistor, as it levels off after a while [2].

This paper proposes an equivalent circuit to describe the measured terminal behavior of a supercapacitor. A method to identify the parameters of the proposed model is presented. The parameters are measured, and the results are discussed to gain a better understanding of the terminal characteristics of the supercapacitor. Finally, some typical transients are measured and the results are compared with the predictions of the model.

The parameters of the proposed model should be determined using measurements at the supercapacitor terminals. To decide the structure of the equivalent circuit, three major aspects of the physics of the DLC should be taken into account. First, based on the electrochemistry of the interface between two materials in different phases, the double-layer capacitance is modeled by a large number of parallel resistive capacitive branches with different time constants. Second, based on the theory of the interfacial tension in the double layer, it can be expected that the capacitance of the device depends on the potential difference. In the practical range of the supercapacitor, the differential capacitance measured experimentally varies linearly with the capacitor voltage. Third, the double-layer capacitor shows certain self discharge. A series inductor may be added for pulse applications, but measurements showed that the inductance is so small (nano Henrys) that it can be neglected in most applications.

For a simple model and the experience from measurements, a model consisting of three RC branches is proposed. This provides three different time constants to model the different charge transfers, which provides sufficient accuracy to describe the terminal behavior of the supercapacitor for the desired span of 30 minutes.

In this paper to show the voltage dependence of the capacitance, the first branch is modeled as a voltage dependent differential capacitor C_{dlff} explained in the next section. The differential capacitor consists of a fixed capacitance C_{iO} and a voltage dependent capacitor C_{il}* V. A resistor, parallel to the terminals, is added to represent the self discharge property. The proposed equivalent circuit is shown in Figure 3.

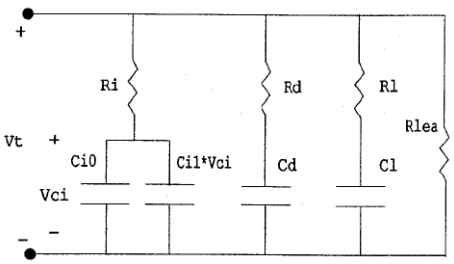


Fig.3:- Equivalent model circuit of supercapacitor

The first or immediate branch, with the elements R_i, C_{iO} and the voltage dependent capacitance C_{il} in [F/V], dominates the immediate behavior of the supercapacitor in the time range of seconds in response to a charge action. The second or delayed branch, with parameters R_d and C_d, dominates the behavior in the range of minutes. Finally, the third or long term branch, with parameters R_l and C_l, determines the behavior for times longer than 10 minutes.

The selection of three branches is the small number, if good accuracy is wanted for the specified time range of 30 minutes. In this model the self discharge resistor is neglected in this time range due to its large value. Each of the three branches has a time constant differing from the other branches usually more than a magnitude. This gives a very practical model, as certain transients can be associate with one of the branches, either: immediate, delayed or long term.

III. PARAMETER CALCULATION OF SUPERCAPACITOR USING CHARGING AND DISCHARGING

The physical property of the supercapacitor gives the idea of a voltage dependent value of capacitance. To understand our model, this property has only been assigned to the first or immediate branch. The relation between voltage and capacitance is described following:

$$C = \frac{Q}{V}$$

Where, Q is the stored charge and V the capacitor voltage. The same definition of C applies if the charge Q is the total charge in the device or an incremental charge ΔQ resulting from an incremental change ΔV in voltage. This definition is not valid for voltage dependent capacitance.

$$C_{diff}(V) = \frac{dQ}{dV}$$

Where, dQ an incremental change in charge at a certain capacitor voltage V that produces an incremental change in voltage dV.

The internal parameters of the supercapacitor model with three RC branches that have heard time constants can be identified carrying out a single fast current controlled charge. It is proposed that the parameters are identified by charging the supercapacitor from zero to rated voltage and by observing the terminal voltage during the internal charge redistribution over the time of 30 minutes. The requirements to achieve actual and repeatable, it is necessary to use a precisely timed and controlled current source to control exactly the provided charge. In addition, the supercapacitor must be in a state where all the model equivalent capacitances have zero voltage, that means any internal charge distribution has stopped and the initial charge stored is known.

Fast controlled charging process is determined by the parameters of the first or immediate branch. After the external charging stops, all charge is in the capacitors of the immediate branch. Then, the charge redistributes itself to the delayed branch without affecting the third or long time branch, which has a much higher time constant. After the voltages in the immediate and delayed capacitors are equalized, the charges start to redistribute to the capacitor of the long term branch.

- Calculation of immediate branch parameters:
  - n=0:
    At that time $V_0 = 0$ V
    $Q_0 = 0$
    Current source is switched on (I = Ich)
  - n=1:
    t1 = 9 sec
    t1 is given at the at which current source is rises to the sat value I_{ch} in 9 sec,
    At that time measure V_1. V_1=1.29 V
    After small time t_1

$$Ri = \frac{V1}{Ich} = 0.645\Omega$$

  - n=2:
    At when $V_2=V_1+\Delta V$
    ΔV chosen to be 500 mV. Measure t_2.
    t_2=62 sec,
    $\Delta t = t_2-t_1 = 53$ sec.
    $C_{io} = Ich\frac{\Delta t}{\Delta V} = 212\ F$

  - n=3:
    Reached when V_3 = V rated. V_3 = 2.4 V.
    Measure t_3. t_3 = 210 sec:
    Now current source is turned off(I_{ch} = 0)

  - n=4:
    $t_4 = t_3 + 9$ sec.
    9 sec is given by fall time of the current.
    At that time measure V_4. V_4 = 1.828 V.
    Total charge supplied to the supercapacitor:
    $Q_{tot} = I_{ch} * (t_4 - t_1)$ = 420 coulomb.
    Now we calculate $C_q = Q_{tot}/V_4$ = 229.75 F.

$$Ci1 = \frac{2}{V4} * \left(\frac{Ich * (t4 - t1)}{V4} - Ci0\right) = 19.43\ F$$

- Calculation of delayed branch parameters:
  - n=5:
    At when $V_5 = V_4 - \Delta V$:

ΔV is chosen to be500 mV. V_5 = 1.328 V.

Measure t_5. t_5 = 303 sec.

$\Delta t = t_5-t_4 = 84$ sec.

As ΔV is small and C_d is assumed dischraged,

$I_{tr} = (V_4 - \Delta V/2)/R_d$.

(R_i is neglected because $R_i << R_d$))

Relating the transfer current $I_{tr} = C_{diff} * \Delta V/\Delta t$.

Here, $C_{diff} = C_{i0} + (C_{i1} * V) = 258.63$ F.

Now,

$$Rd = \frac{(V4 - \frac{\Delta V}{2} * \Delta t)}{Cdiff * \Delta V} = 1.025\Omega$$

- n=6:
  $t_6 = t_5 + 3(R_d * C_d)$

  Typically $R_d * C_d = 20$ sec. $t_6 = 303$ sec

  Measure V_6. $V_6 = 1.164$ V.

$$Cd = \frac{Qtot}{V6} - \left(Ci0 + \frac{Ci1}{2} * V6\right) = 137.51\ F$$

➢ Calculation of long term branch parameters:

- n=7:
  At when $V_7 = V_6 - \Delta V$. $V_7 = 0.664$ V.

  Measure $\Delta t = 73$ sec:

  As ΔV is small and C_l is assumed discharge, I_{tr} is virtually constant and given by:

$I_{tr} = (V_6 - \Delta V/2)/R_l$.

(R_i and R_d neglected because$R_i << R_d << R_l$).

Because R_d is much larger than R_i, the transfer current I, at this initial instant is supplied mainly from the immediate branch:

$I_{tr} = C_{diff} * \Delta V/\Delta t$.

$$Rl = \frac{(V6 - \frac{\Delta V}{2} * \Delta t)}{Cdiff * \Delta t} = 5.9\Omega$$

- n=8:
  $t_8 = 30$ min:

  At t, it is assumed that the charge redistribution to the long term branch has ended and the three equivalent capacitors have the same voltage.

  Measure V_8. $V_8 = 0.60$ V.

The long term capacitor (C_l) is calculated using the charge balance:

$$Cl = \frac{Qtot}{V8} - \left(Ci0 + \frac{Ci1}{2} * V8\right) - Cd = 344.66\ F$$

With the clear definition of the procedure for the parameter calculation, the parameters values may now be measured. The following table summarizes the average results of the parameters measurements:

PARAMETERS	540 F supercapacitor
R_i	0.645 Ω
C_{i0}	212 F
C_{i1}	19.43 F
R_d	1.025 Ω
C_d	137.51 F
R_l	5.9 Ω
C_l	344.66 F
R_{leak}	1.6 KΩ

Above calculation is calculated from following charging and discharging graph. The experimental graph voltage verses time for Charging and discharging (at constant current applying 2 amp) are given below. Which is clearly mention that voltage is increasing with time and capacitor is charge and voltage is decreasing with time when capacitor is discharge.

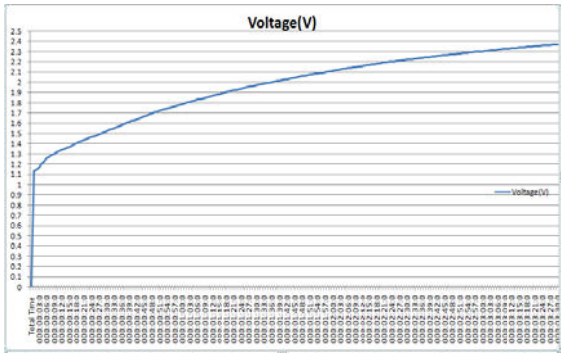
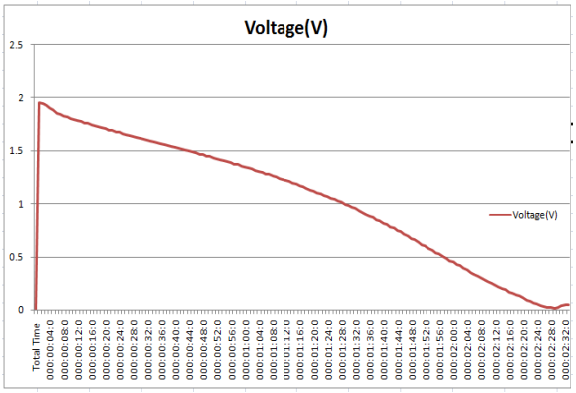


Fig.4:-Charging of supercapacitor with constant current 2 A.

Figure 4 shows the terminal voltage during the charge action with constant current and the first minutes of the internal charge distribution process. This graphic presents the first three minutes of the capacitor response to a charge action. In other words, the figure compares the experimental results with the simulation during the time that the immediate and delayed branches predominate in the capacitor behavior.

Figure 5 shows terminal voltage during recharge action with constant current. After that, the capacitor is discharged until the voltage across the immediate and delayed branches are at approximately equal. Finally, the current is turned off again and the change in terminal voltage thereafter is very low since that change is given only by the long term branch.



Fig,5: Discharging of supercapacitor with constant current 2A.

IV. SIMULATION OF INTERNAL PARAMETERS OF SUPERCAPACITOR USING MATLAB

The software to be used for simulation is MATLAB. In this simulation tool, the system to be simulated is represented by the differential equations that govern the response of the system. In addition, the program gives a graphical output of the state variables and any other variable previously defined. Fig.6 shows the simulation model of supercapacitor.

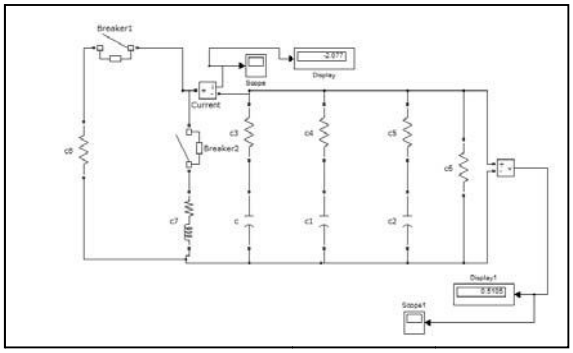


Fig.6: Simulation model of supercapacitor.

Fig.7 shows the charging graph of simulated model. That gives comparison of experimental graph and simulated graph. This graph represents the capacitor response to a charge action. Fig.8 shows the discharging graph of simulated model. In other words, the figure compares the experimental results with the simulation during the time that the immediate and delayed branches predominate in the capacitor behavior. The experimental and simulated results are in a very good agreement with each other. This graph shows the time constant of immediate branch is few seconds and delayed and long term branch is very high in minutes.

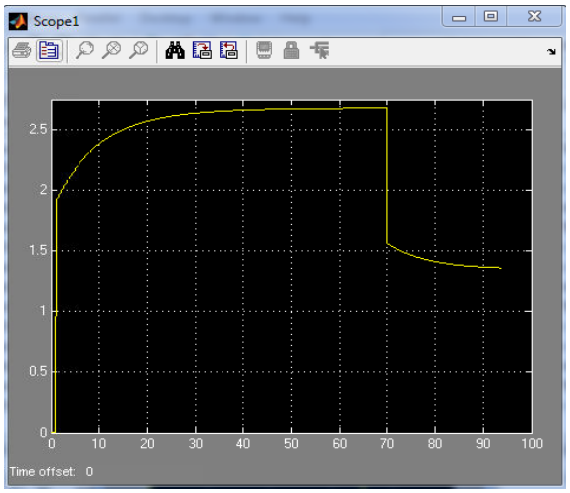


Fig.7:-Charging graph of simulated model.

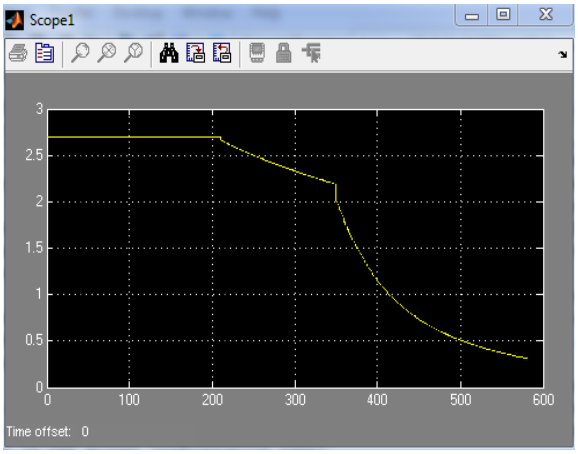


Fig.8:-Discharging graph of simulated model.

V. CONCLUSION

The model gives the internal charge distribution process very well within the considered time span. The internal parameters of supercapacitor can be calculated from this experimental and simulation model. And the exact behavior of the supercapacitor can be predicted form this data. Based on this data the supercapacitor can be selected for any particular application in power system. The studies of simulated model and experimental data of supercapacitor suggest the application in power electronics.

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